

MODEL NAME : *AAM00*
PCB NO : *LA-C361P*

BOM P/N :

Dell/Compal Confidential

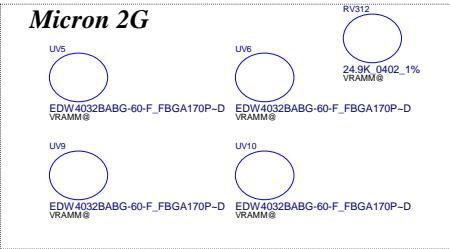
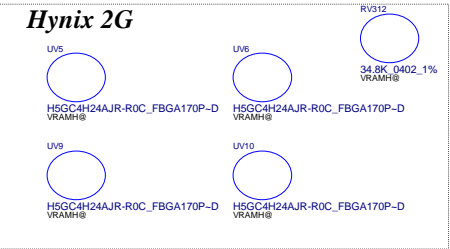
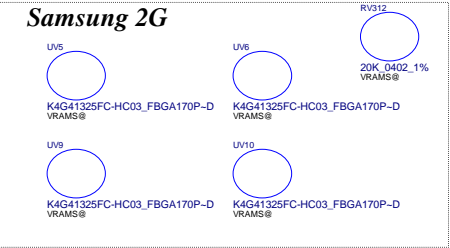
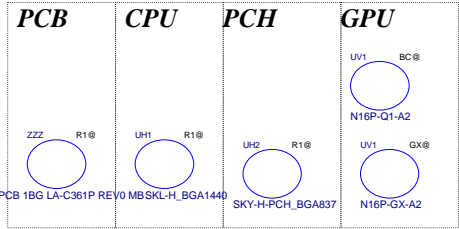
Schematic Document

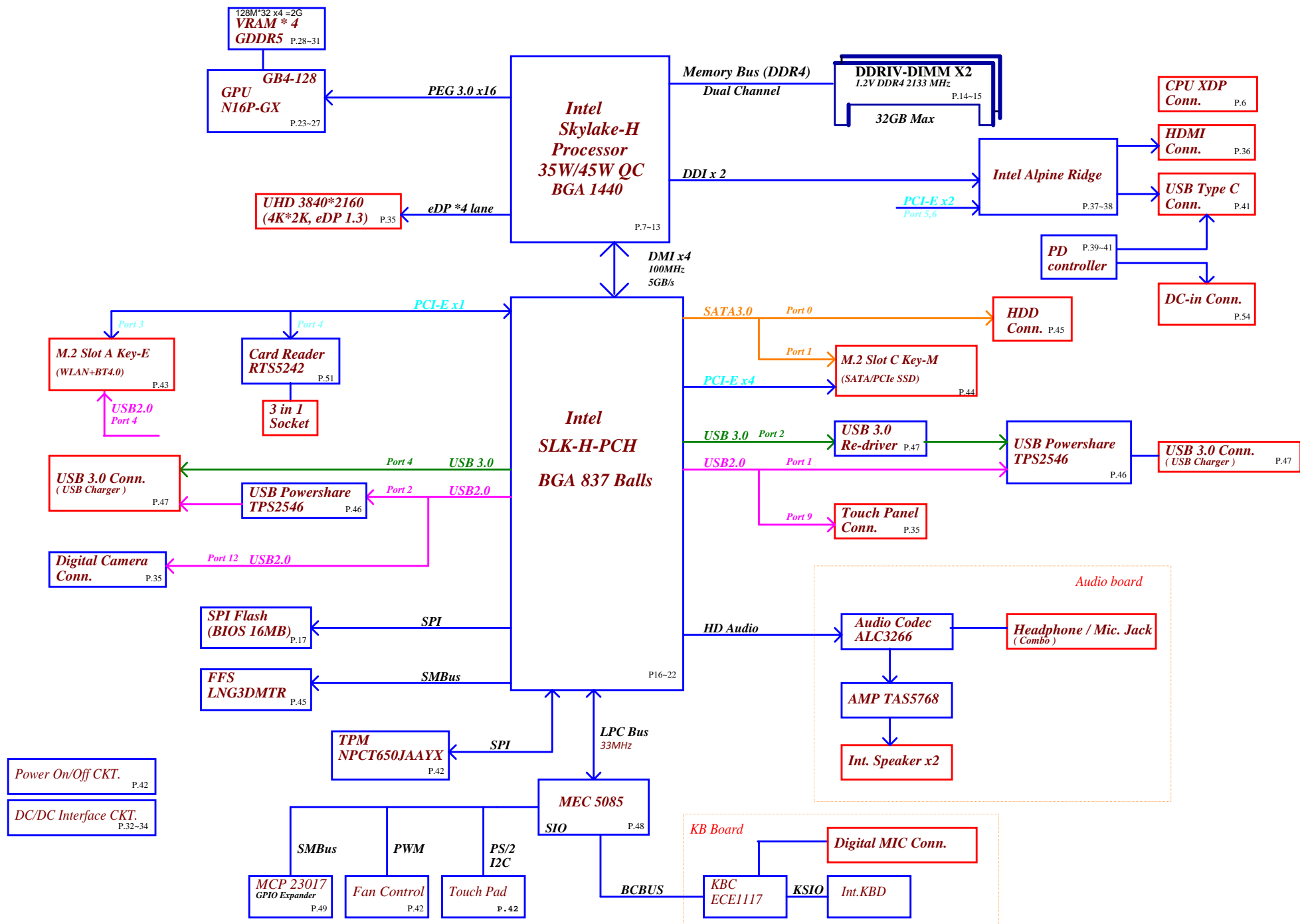
SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

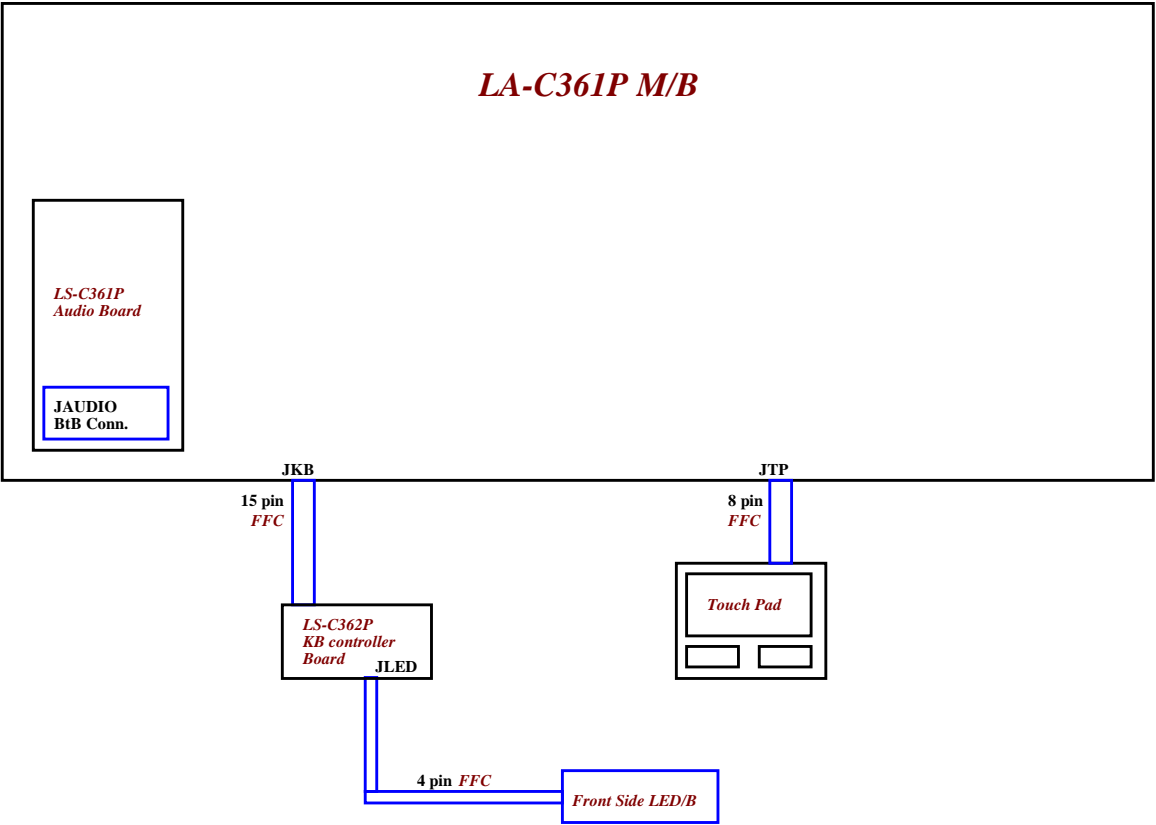
@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
TPM@ : TPM function
EMC@ : Pop of EMI parts
VRAMS@ : Samsung GDDR5 for GPU
VRAMH@ : Hynix GDDR5 for GPU
VRAMM@ : Micron GDDR5 for GPU
BreakDown@ : for measure power consumption
CSMB@ : CSMB sku
BC@ : BC sku (GPU N16P-Q1)
GX@ : GPU N16P-GX
UMA@ / DIS@ : UMA/DIS





Compal Confidential

Project Code : AAM00
File Name :



Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA



DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

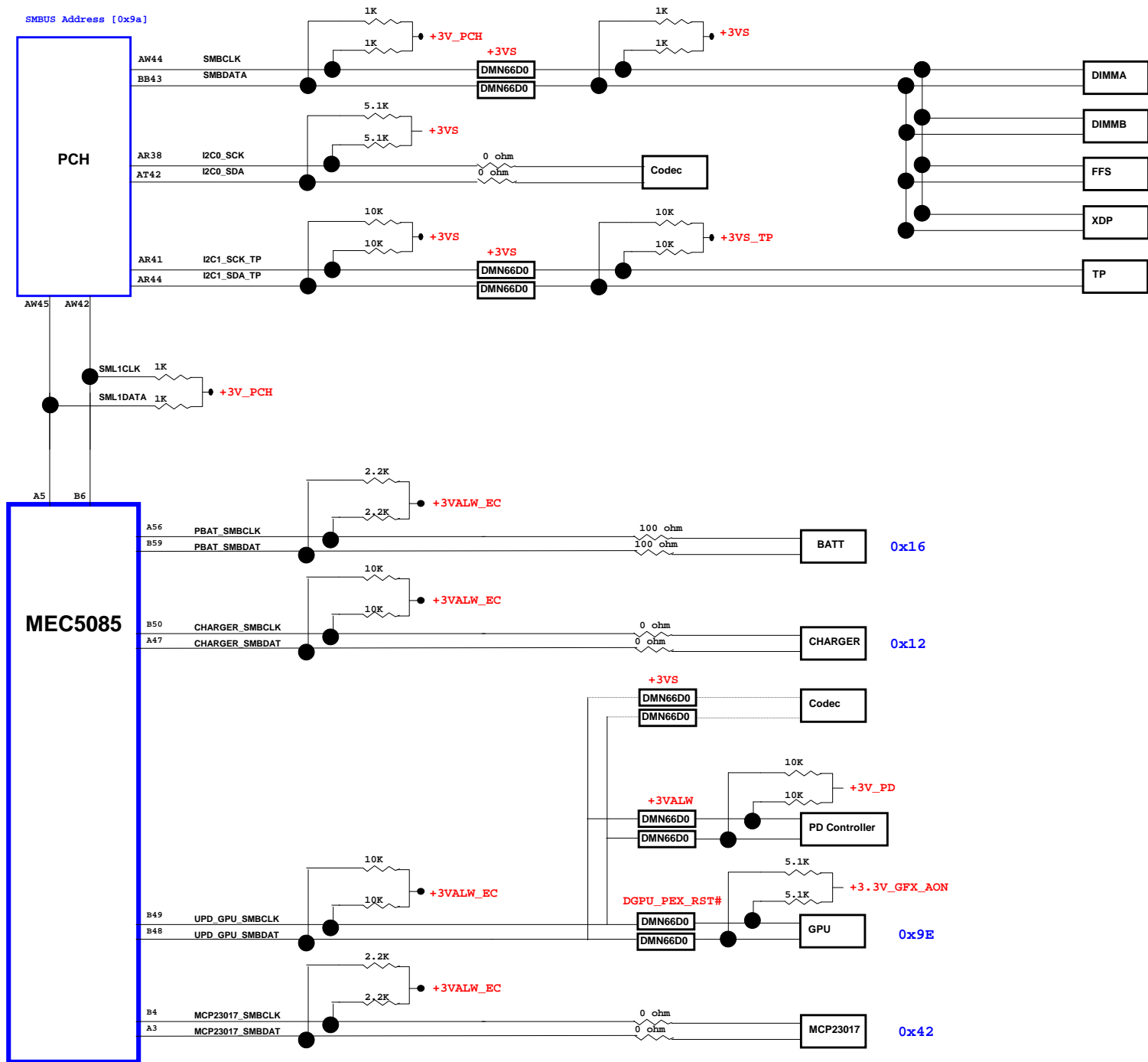
LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

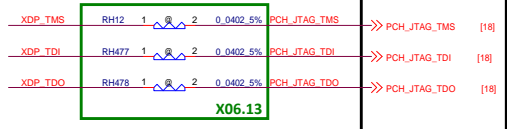
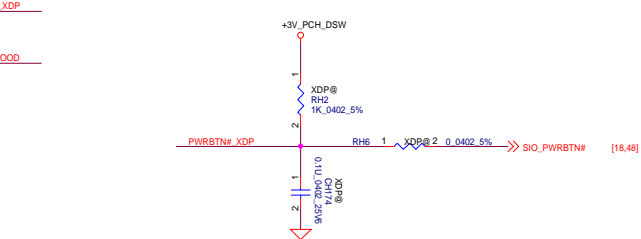
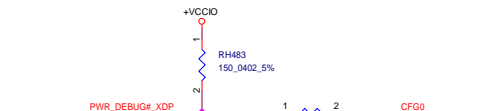
PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD	SATA	DESTINATION
Lane 10	SSD	0A	SSD
Lane 11	SSD	1A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	SSD	N/A	N/A
Lane 14	SSD	0B	None
Lane 15	SSD	1B	HDD
Lane 16	Alpine Ridge	2	None
		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

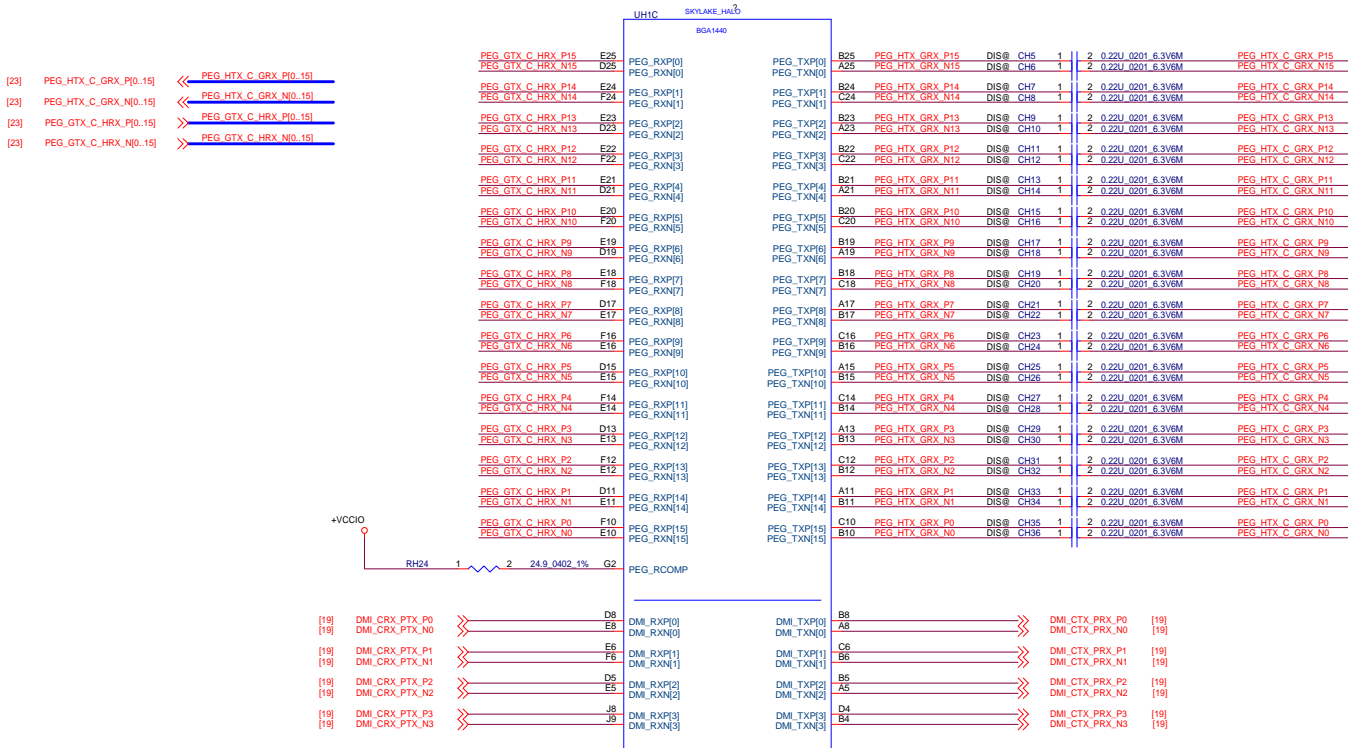
Symbol Note :

 : means Digital Ground
  : means Analog Ground



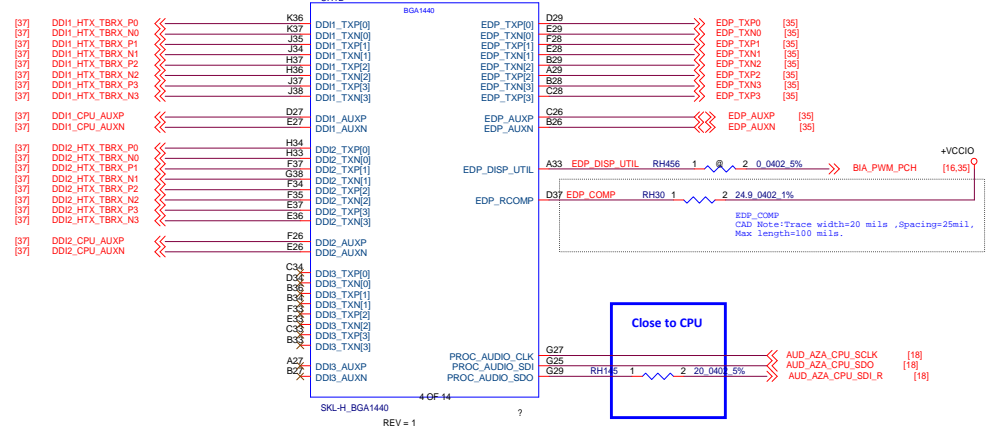


Security Classification		Compal Secret Data		Compal Electronics, Inc. NDP CONN	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND PROPRIETARY INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPANY OR DIVISION OF COMPAL ELECTRONICS, INC. TO ANY OTHER PERSON OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date:	Thursday, August 06, 2015
				Sheet	6 of 71



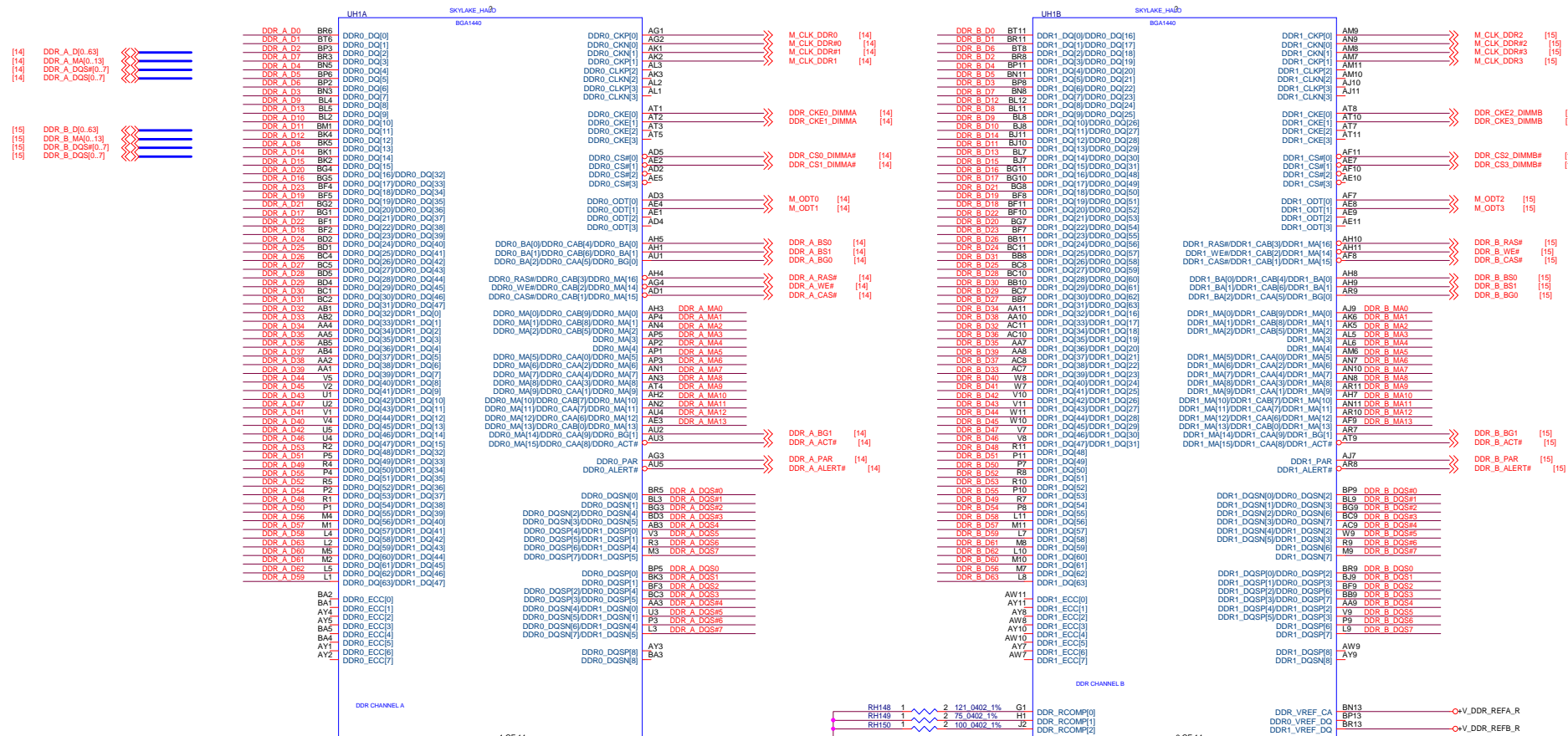
(19) DMI_CRX_PTX_P0
(19) DMI_CRX_PTX_N0
(19) DMI_CRX_PTX_P1
(19) DMI_CRX_PTX_N1
(19) DMI_CRX_PTX_P2
(19) DMI_CRX_PTX_N2
(19) DMI_CRX_PTX_P3
(19) DMI_CRX_PTX_N3

(19) DMI_CTX_PTX_P0
(19) DMI_CTX_PTX_N0
(19) DMI_CTX_PTX_P1
(19) DMI_CTX_PTX_N1
(19) DMI_CTX_PTX_P2
(19) DMI_CTX_PTX_N2
(19) DMI_CTX_PTX_P3
(19) DMI_CTX_PTX_N3



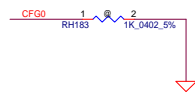
Close to CPU

Interleave

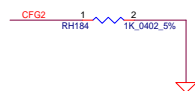


CFG Straps for Processor

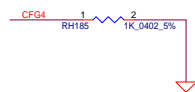
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



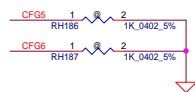
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>★ 0: Lane Reversed</p>



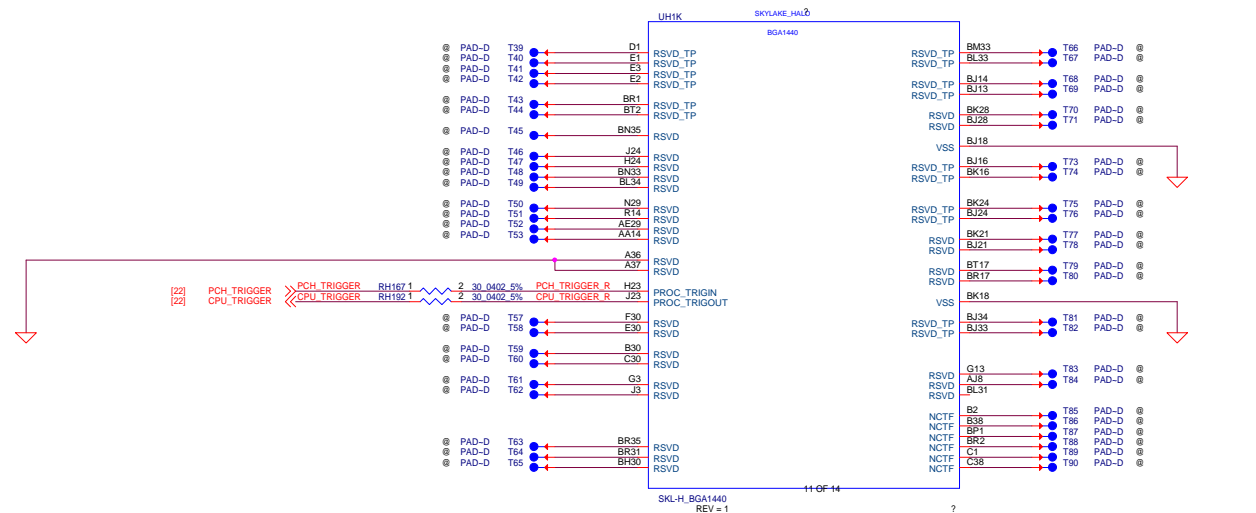
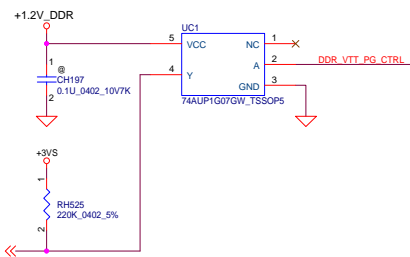
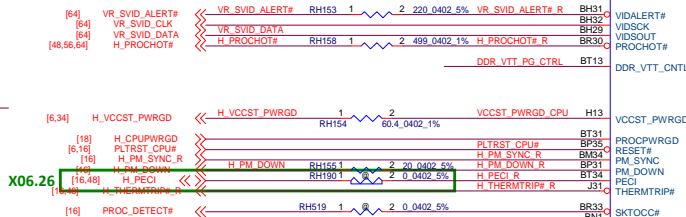
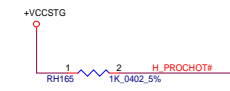
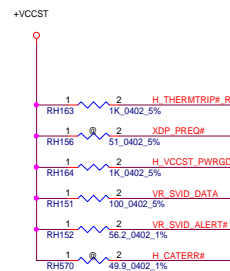
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



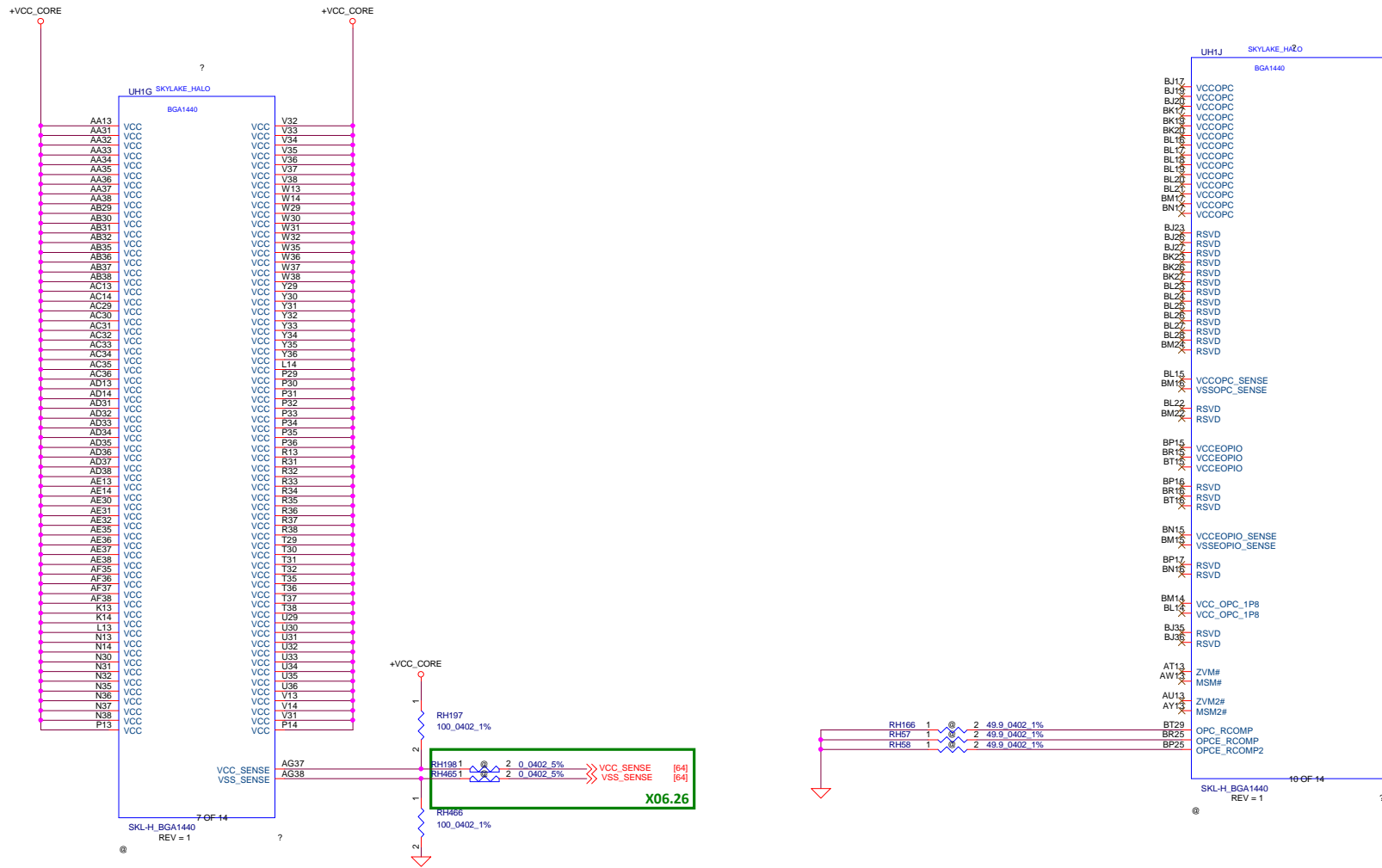
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



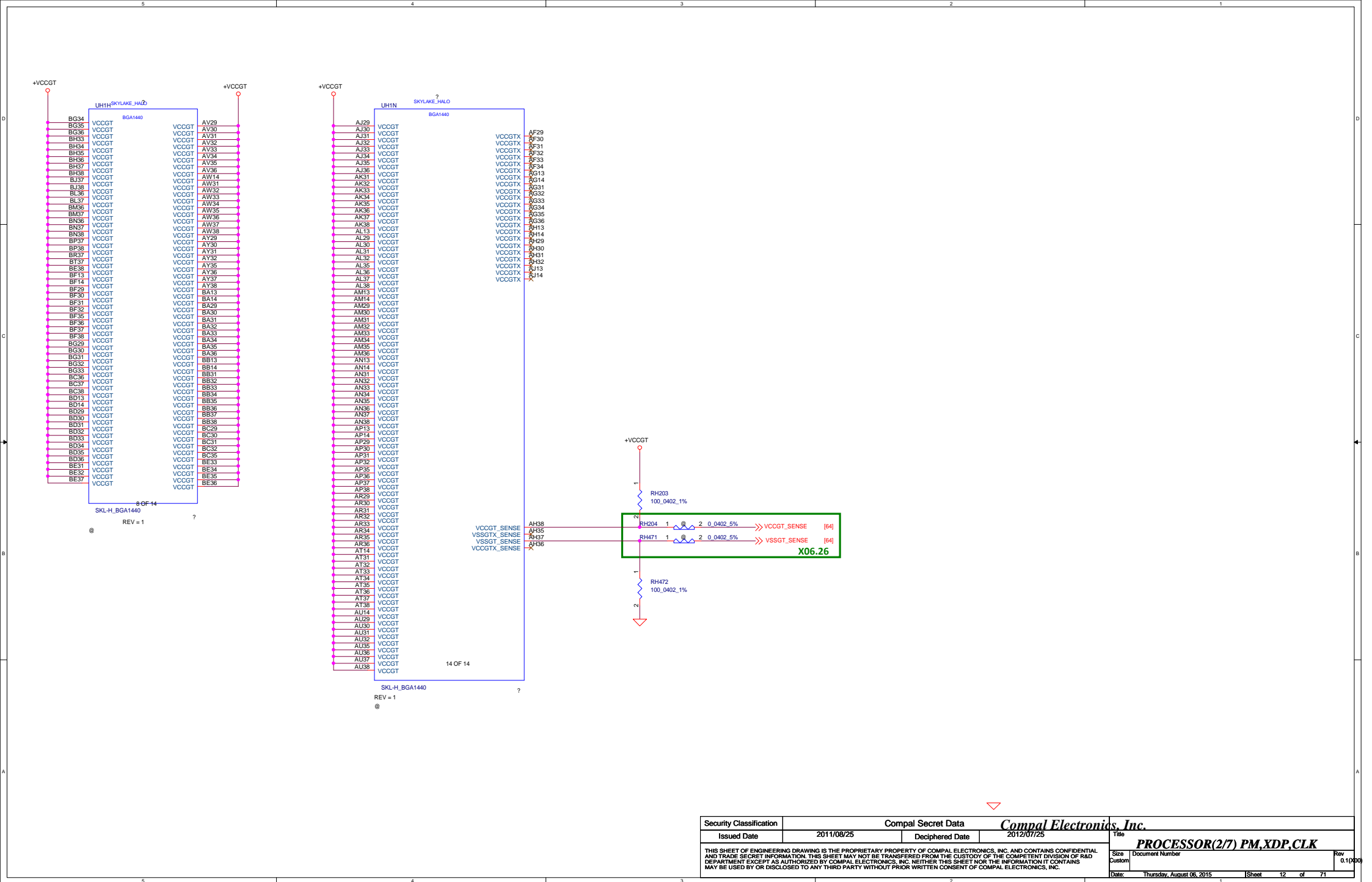
PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



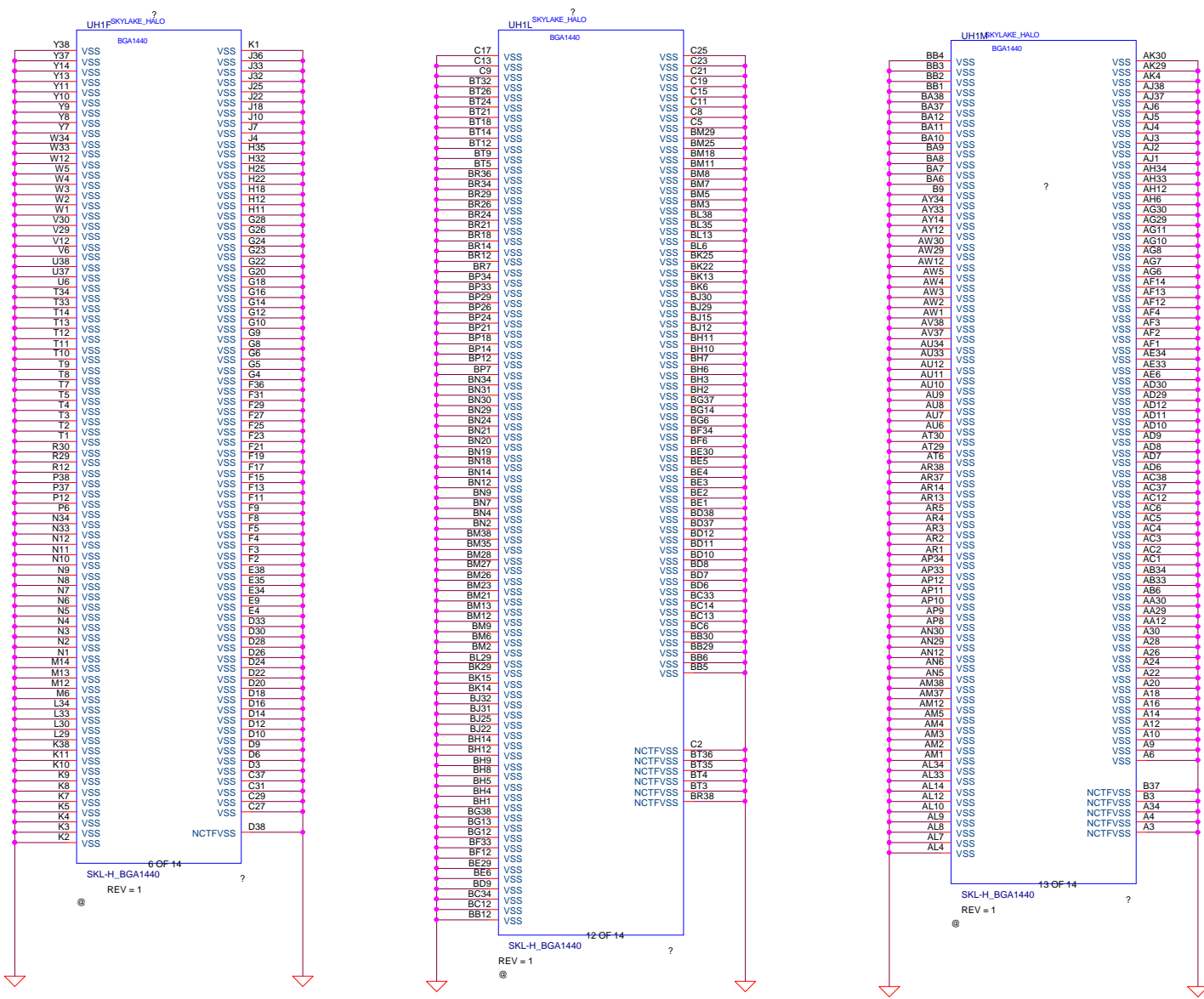
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>				
Issued Date		2011/08/25	Deciphered Date		2012/07/25	Title		
						PROCESSOR(47) RSVD.CFG		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size	Document Number	Rev
						C		0.1(000)
						Date:	Thursday, August 06, 2015	Sheet



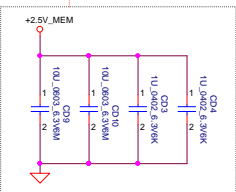
Security Classification	Compal Secret Data			Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	PROCESSOR(5/7) PWR,BYPASS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1(000)
Date: Thursday, August 06, 2015				Sheet 10 of 71	



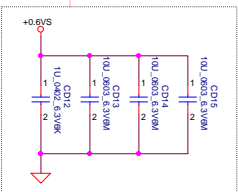
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(2/7) PM,XDP,CLK
Size Custom		Document Number		Rev 0.10000
Date: Thursday, August 06, 2015		Sheet 12 of 71		



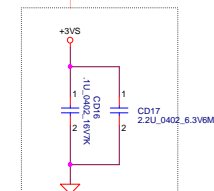
Layout Note:
Place near JDIMM1.257,259



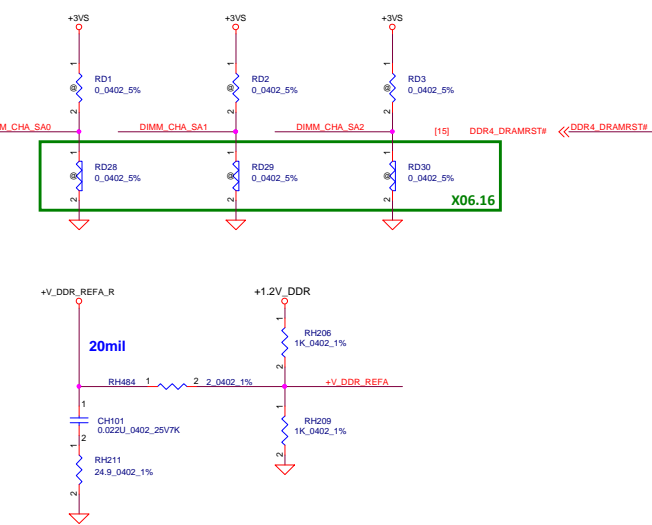
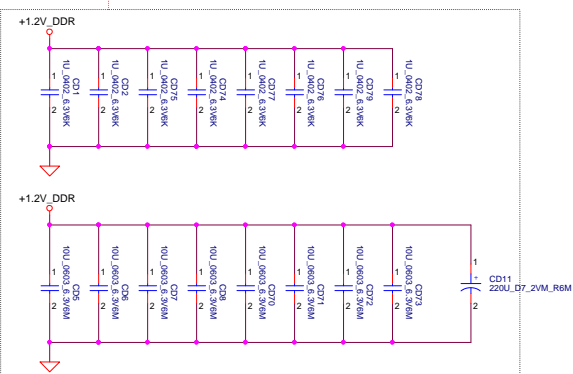
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1.255



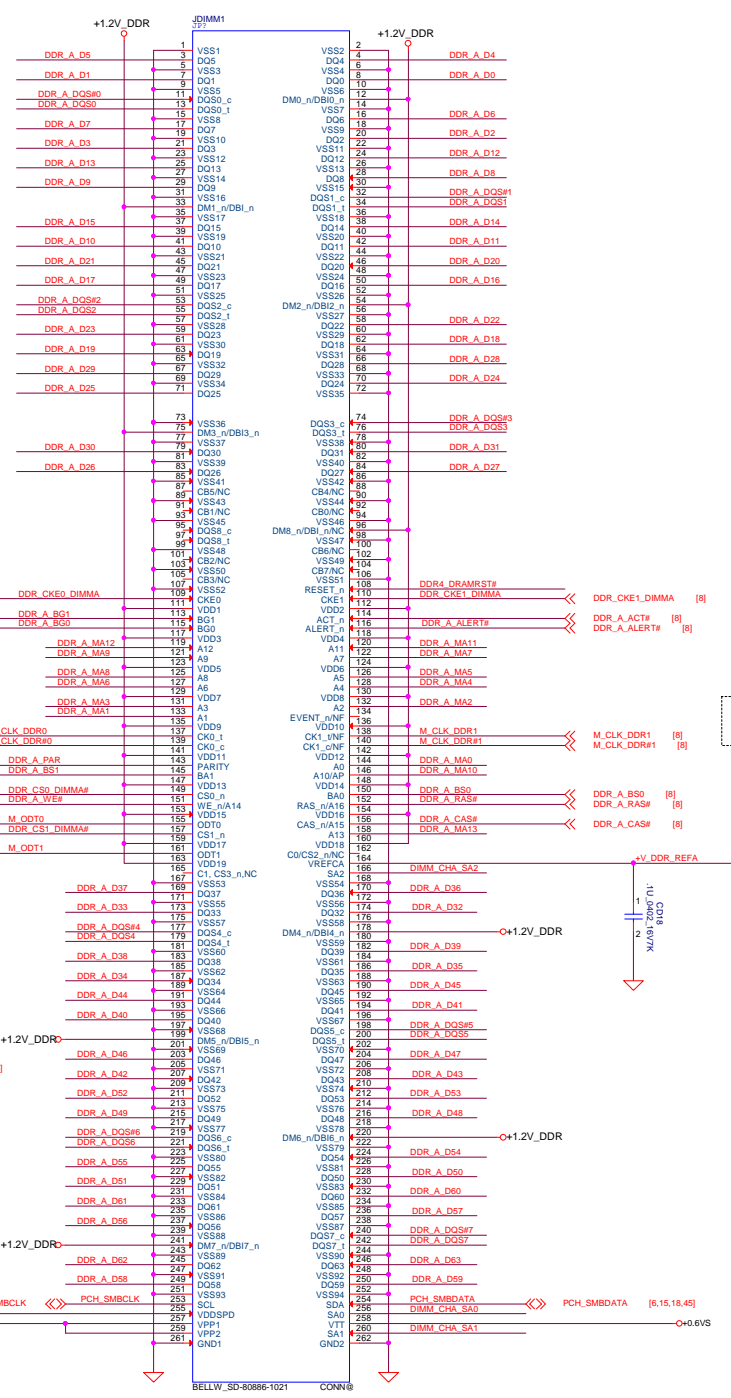
Layout Note:
Place near JDIMM1



X06.12

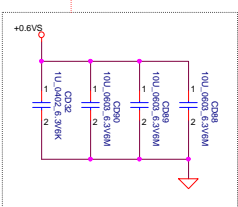
X06.16

[8] DDR_A_D0..[3]
[8] DDR_A_MA0..[13]
[8] DDR_A_DQ3[0..7]
[8] DDR_A_DQ3[0..7]

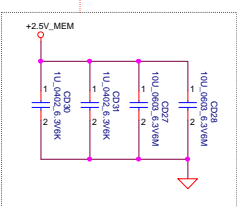


All VREF traces should
have 10 mil trace width

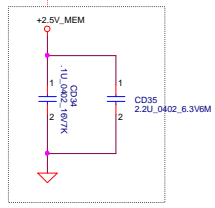
Layout Note:
Place near JDIMM1.258



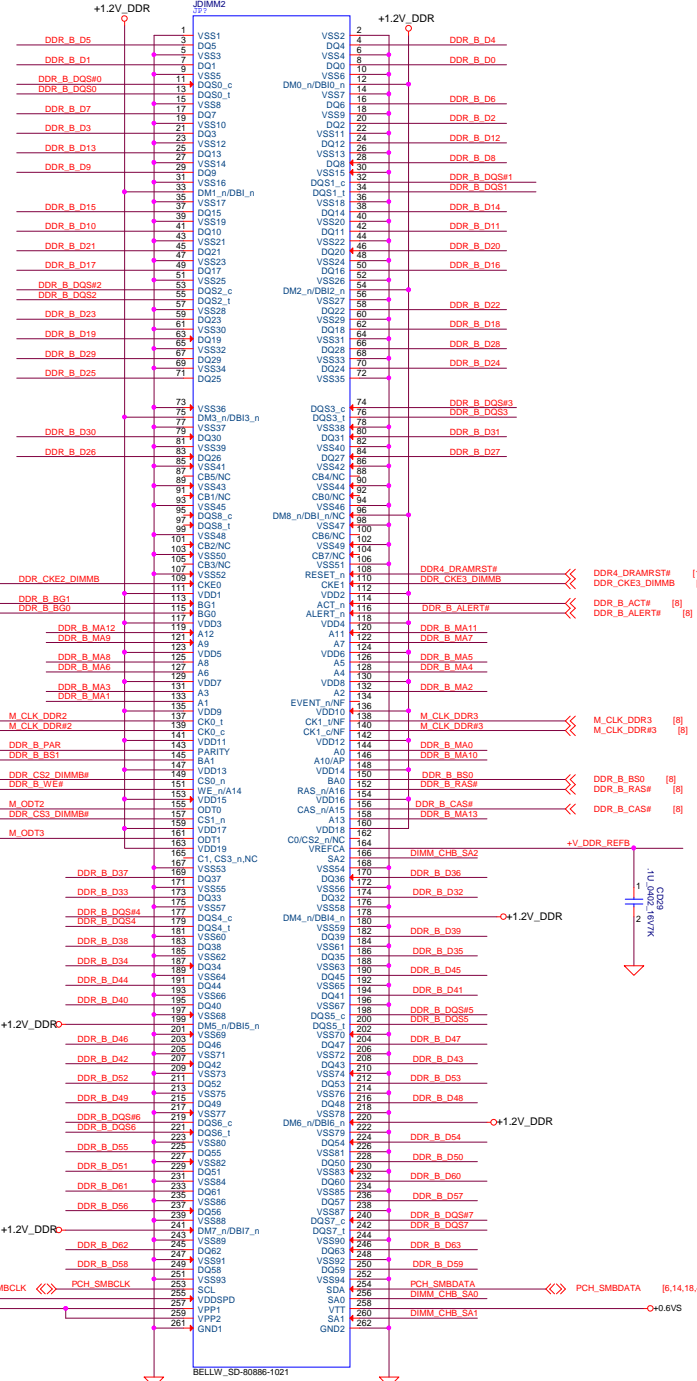
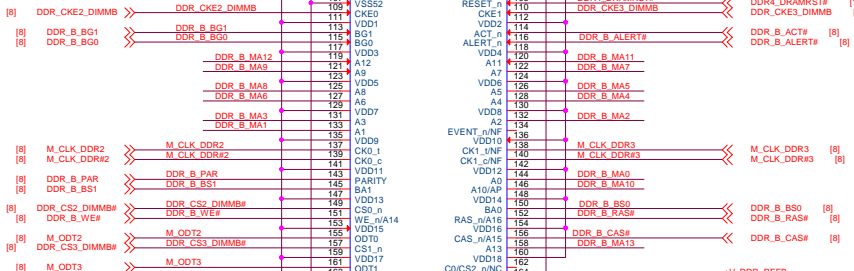
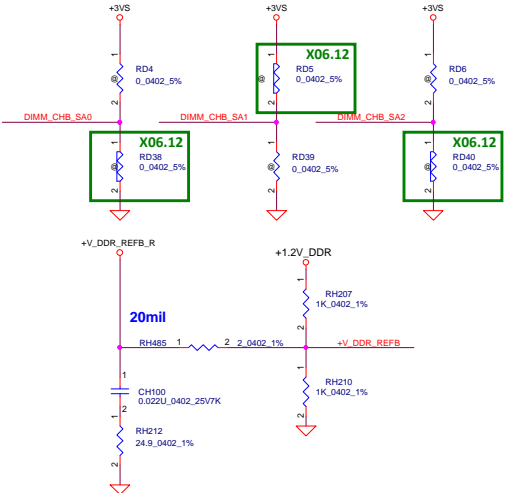
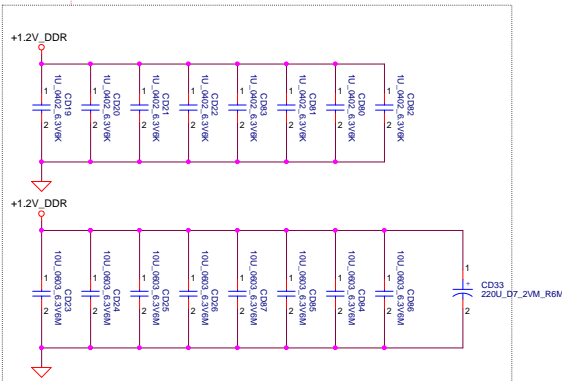
Layout Note:
Place near JDIMM2.257,259



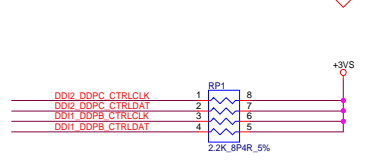
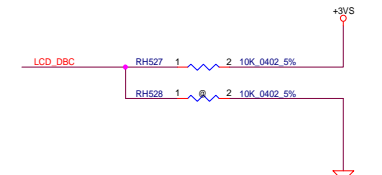
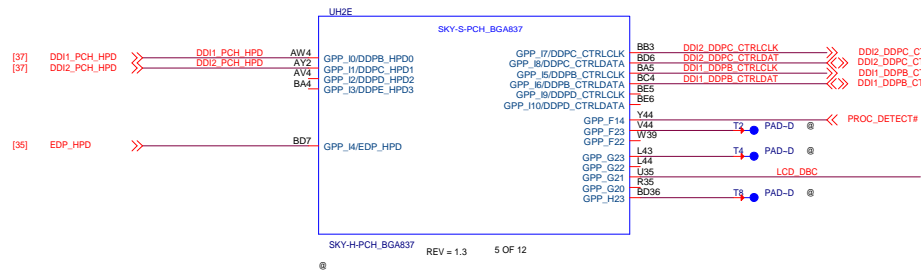
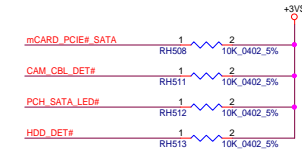
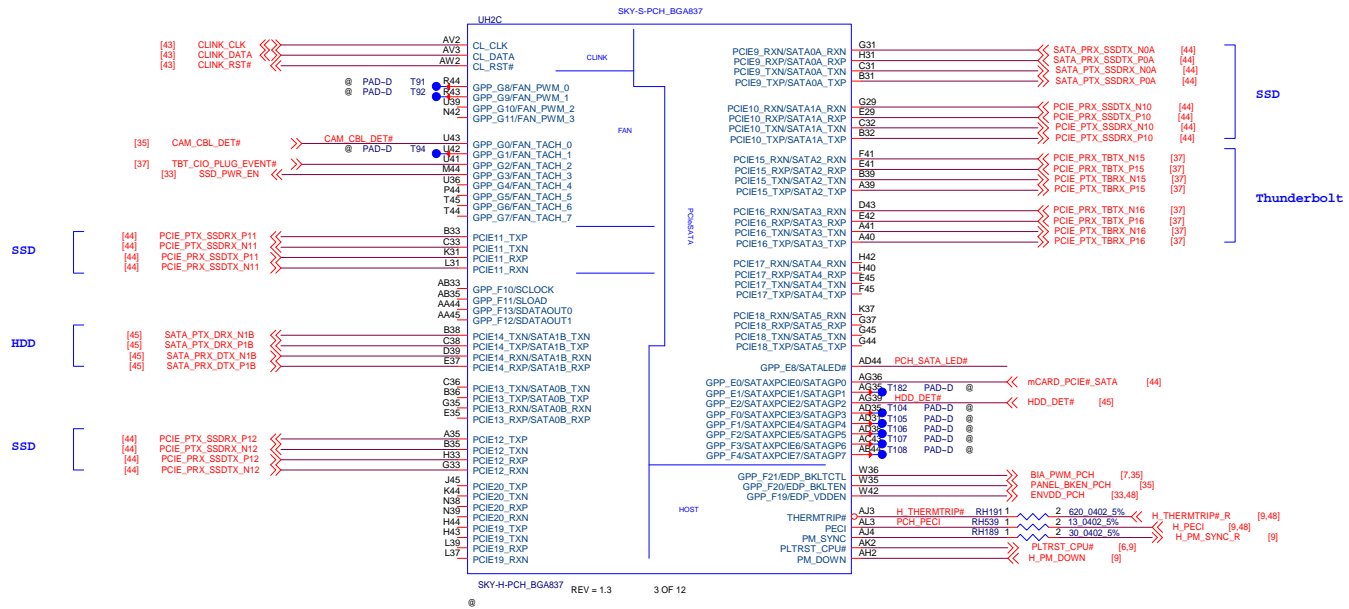
Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMMB



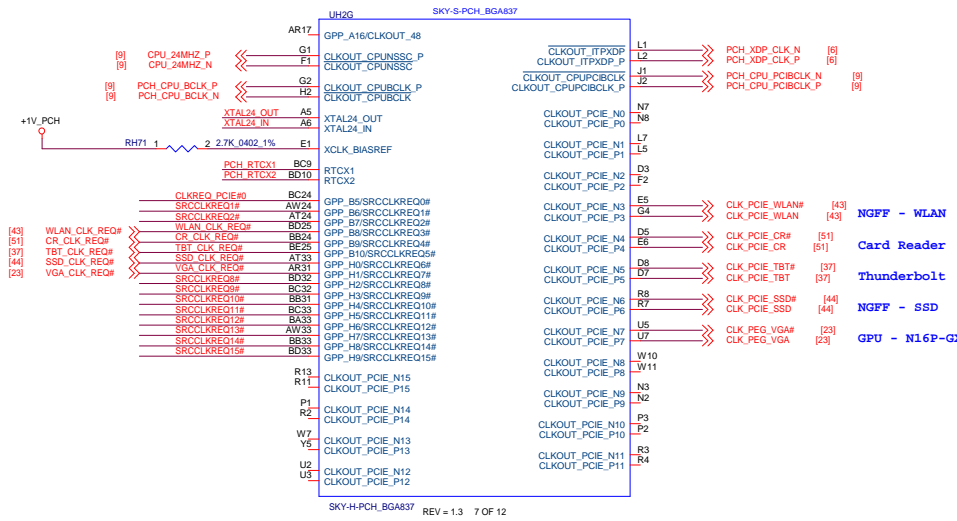
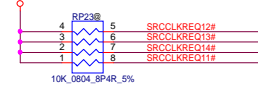
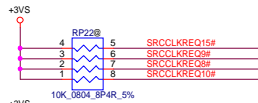
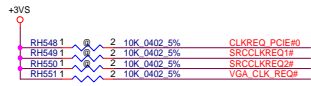
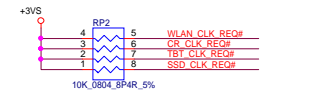
All VREF traces should
have 10 mil trace width



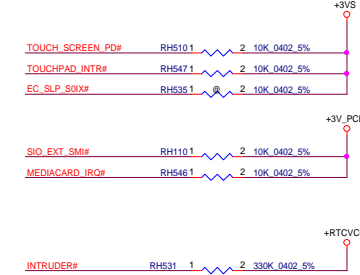
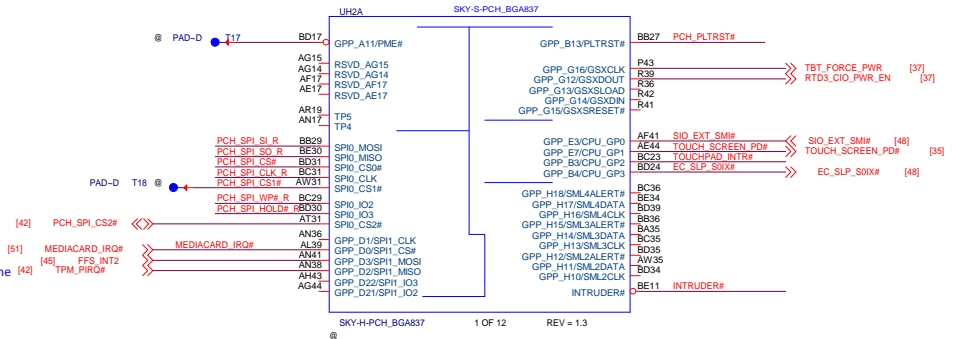
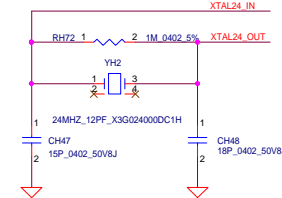
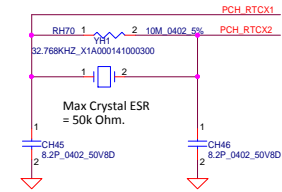
PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	D0PB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	D0PC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	D0PD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

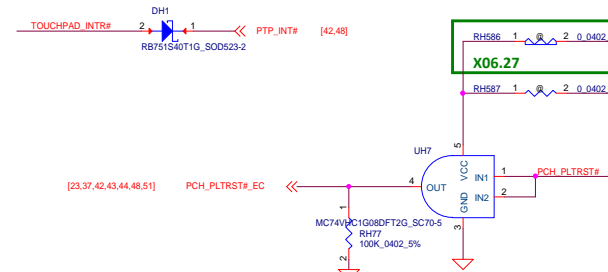
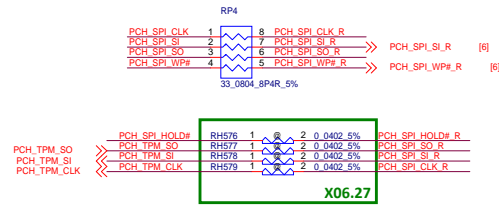


RTC CRYSTAL



9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

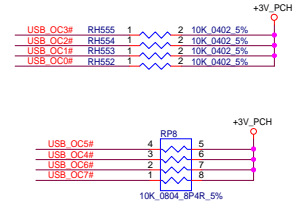
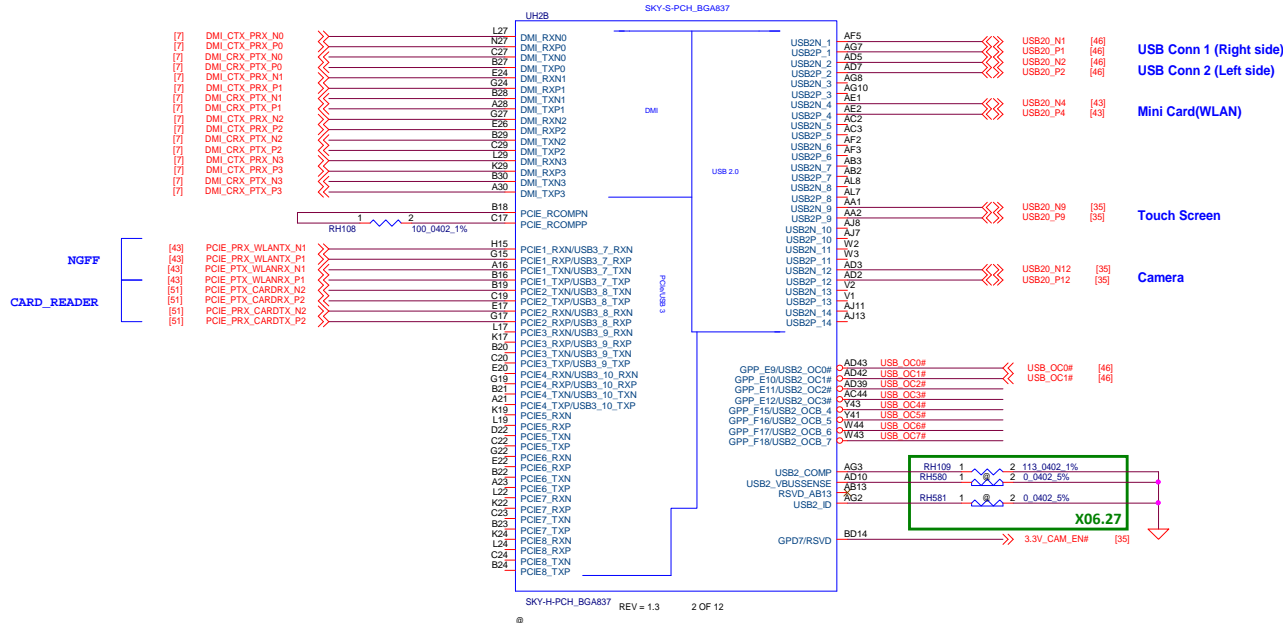
Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-E51/E51 samples.



SPI ROM FOR ME (16MByte)

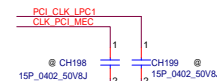
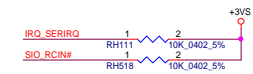
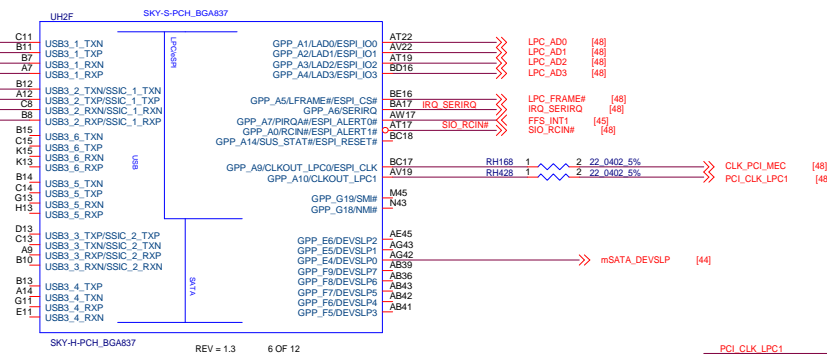


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-C361P
				Size
				17 of 71
				Rev
				0.1(xxx)
				Date
				Thursday, August 06, 2015

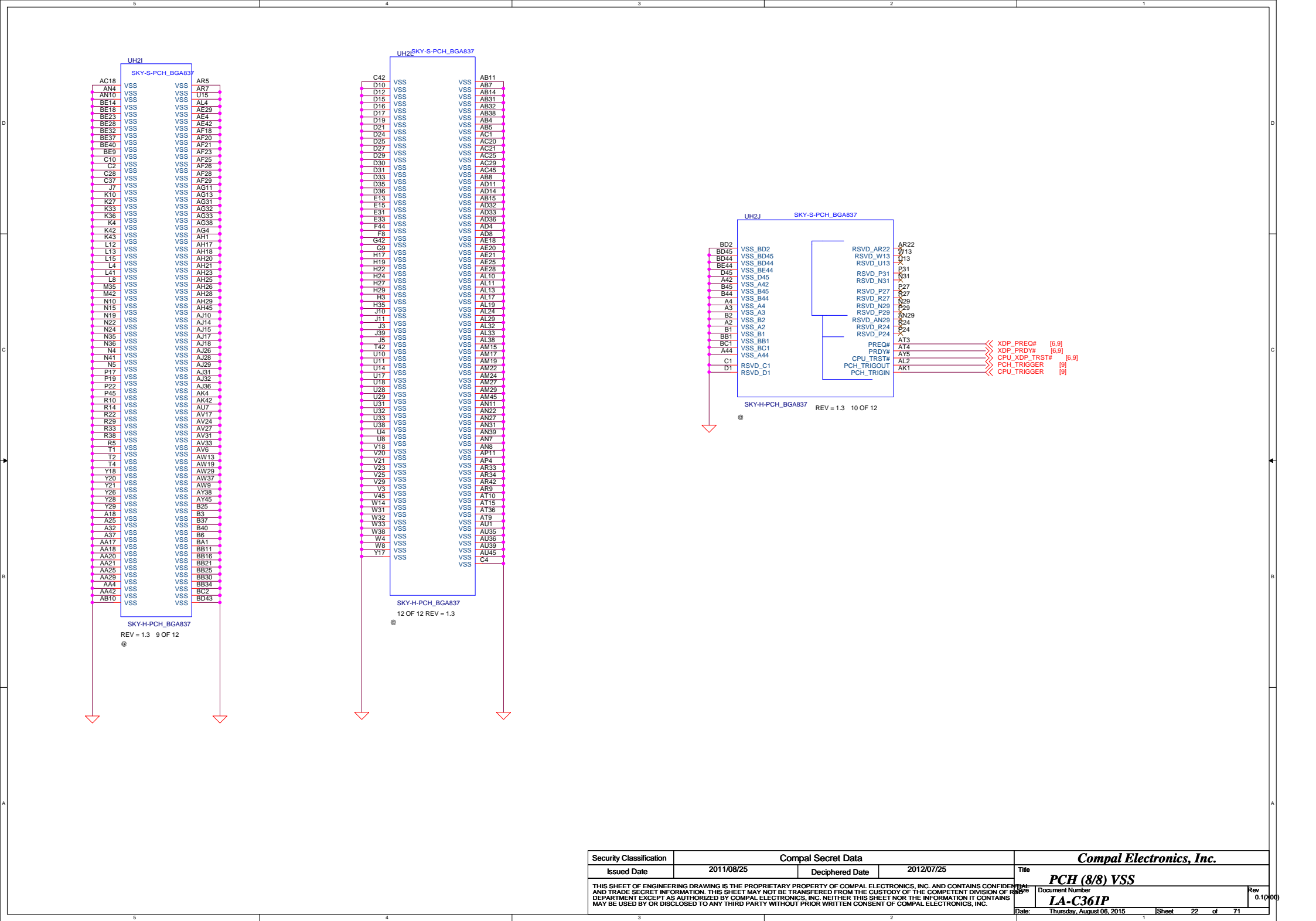


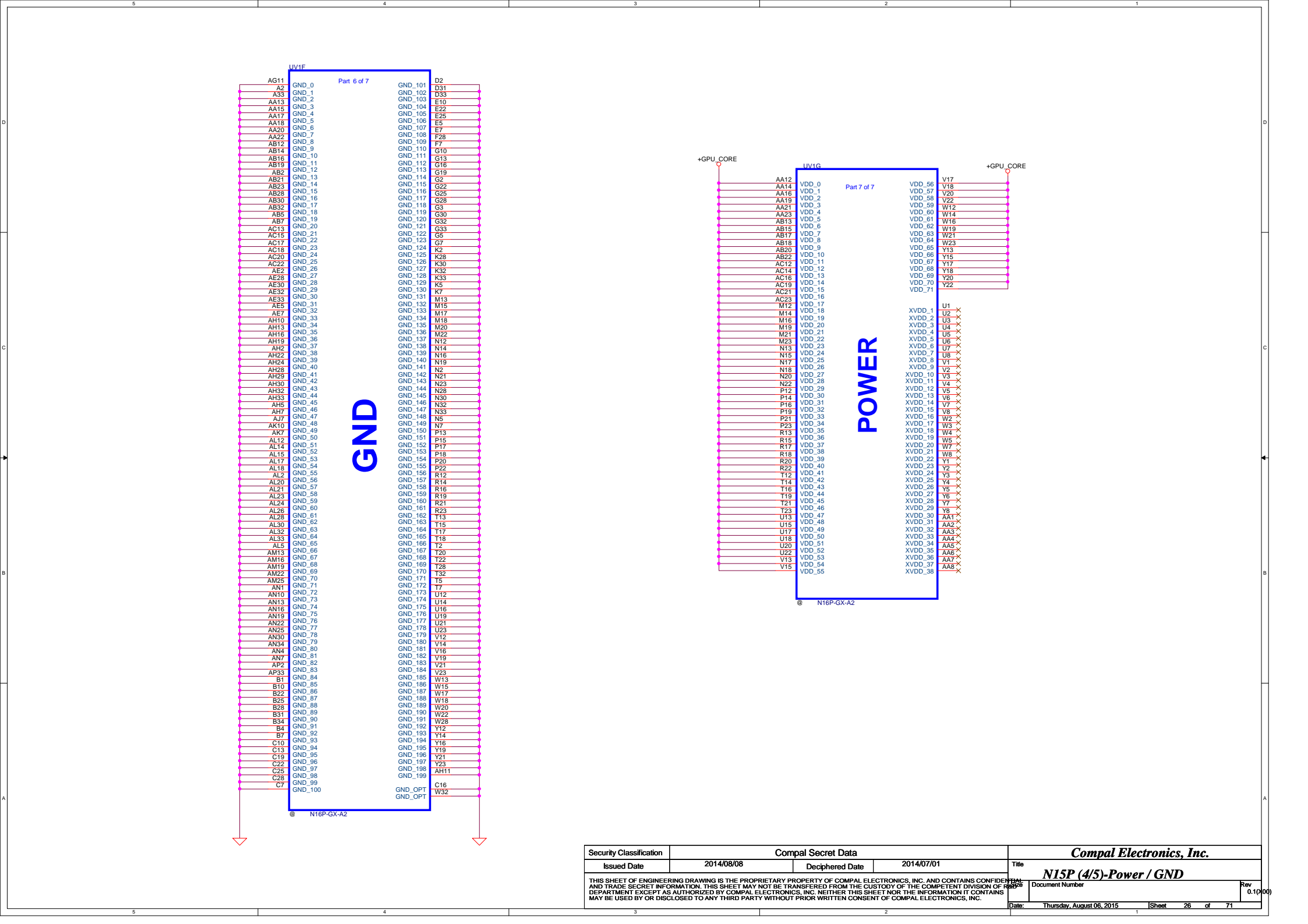
USB Conn 1 (Right Side)
 USB3TN1 [47]
 USB3TP1 [47]
 USB3RN1 [47]
 USB3RP1 [47]

USB Conn 2 (Left Side)
 USB3TN2 [47]
 USB3TP2 [47]
 USB3RN2 [47]
 USB3RP2 [47]

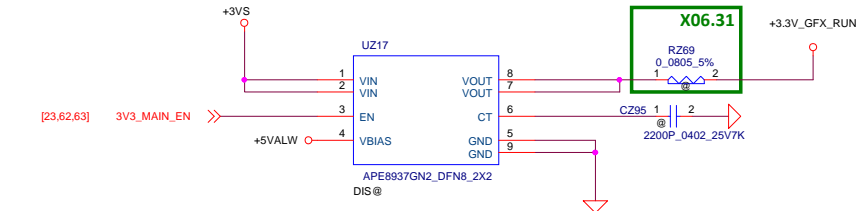


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/08/25		2012/07/25		PCH (4/8) PCL USB	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	
		1		LA-C361P	
		Date		Thursday, August 06, 2015	
		Sheet		19 of 71	

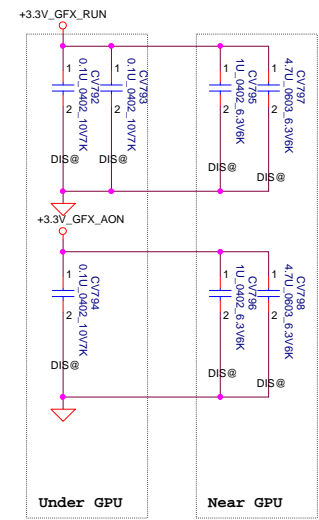
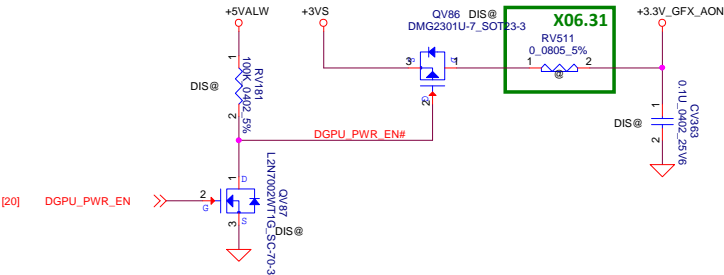




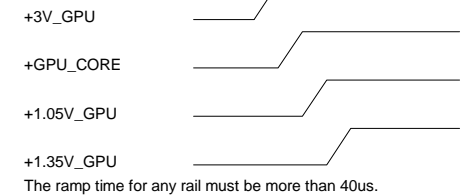
+3.3V_GFX_RUN



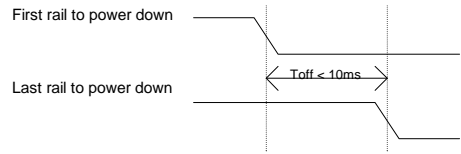
+3VALW to +3.3V_GFX_AON



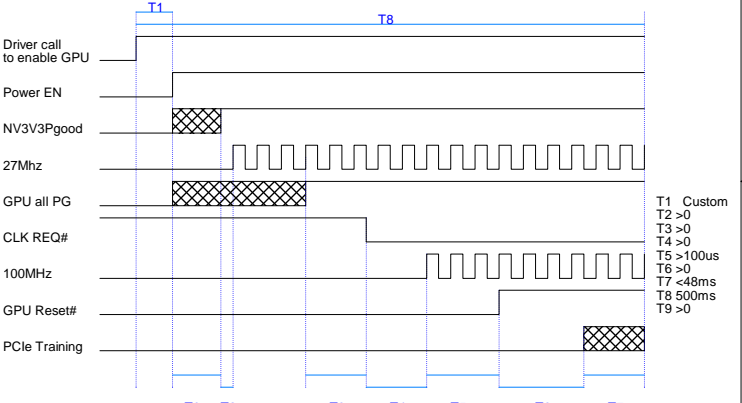
GPU Power Up Power Rail Sequence



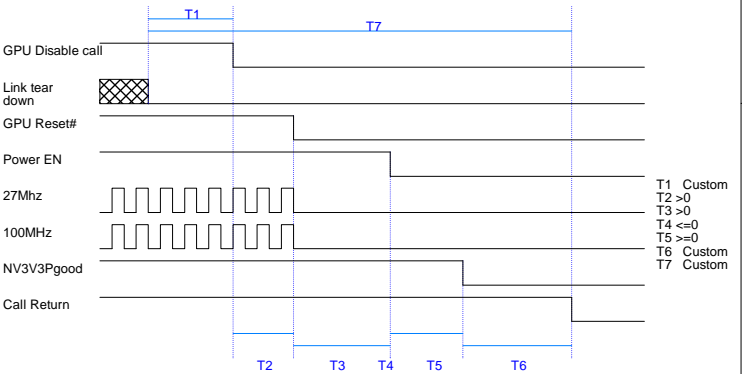
GPU Power Down Sequence



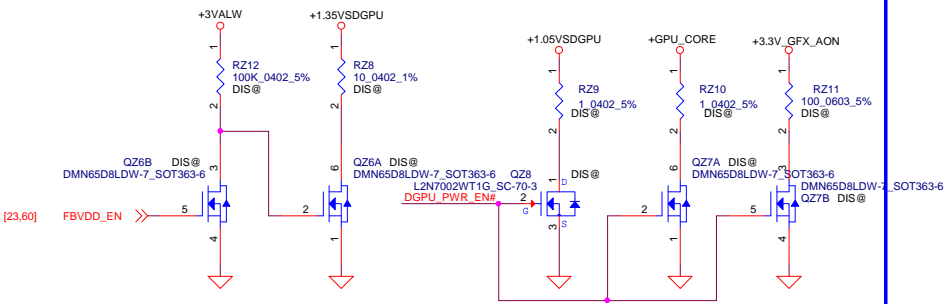
GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence

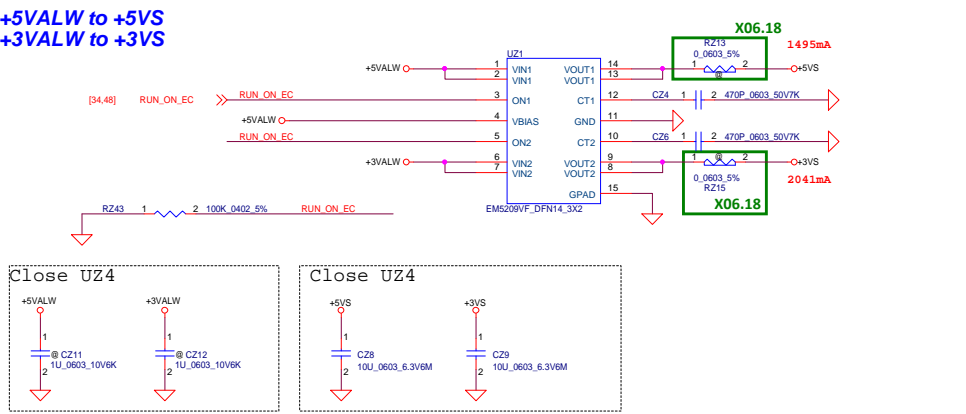


Discharge

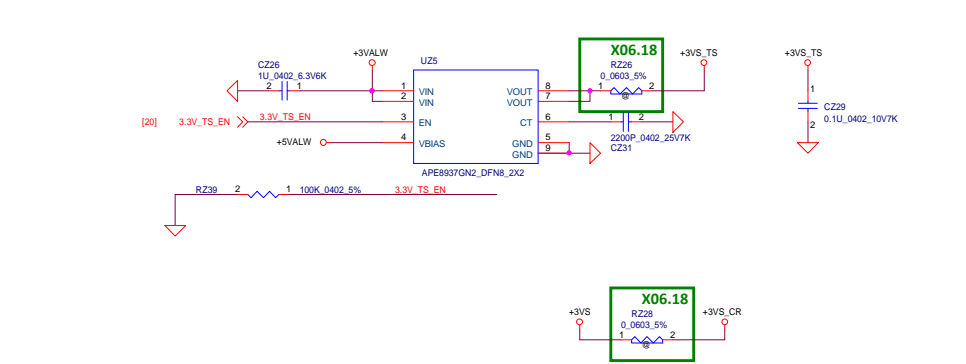


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	GPU DC/DC interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1(100)
				Date: Thursday, August 06, 2015	Sheet 32 of 71

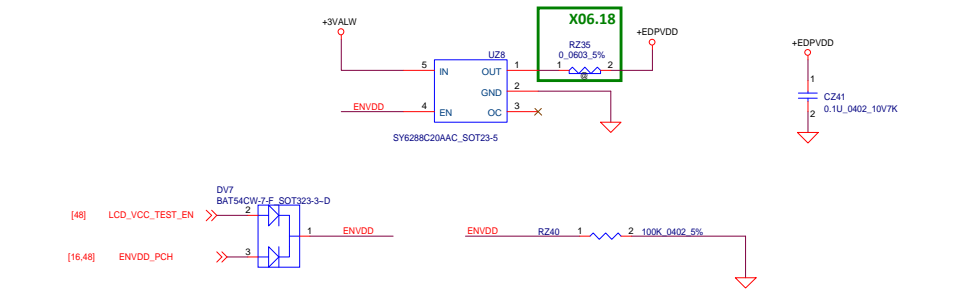
+5VALW to +5VS
+3VALW to +3VS



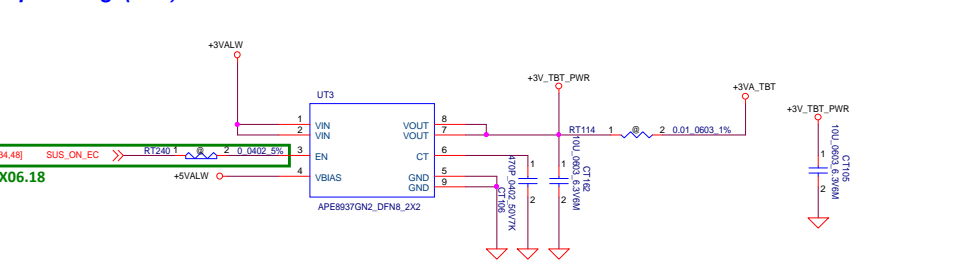
Touch Screen Load Switch & Card Reader



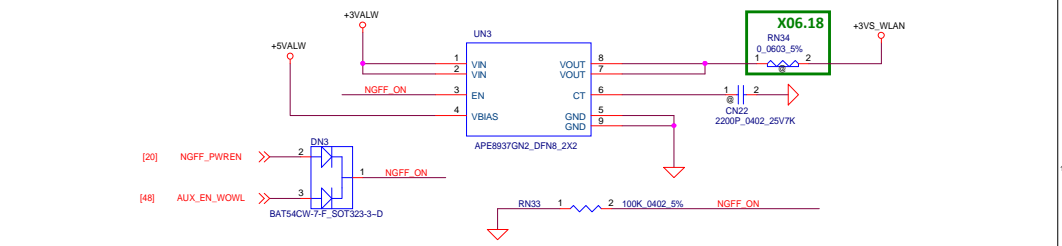
eDP & Camera Load Switch



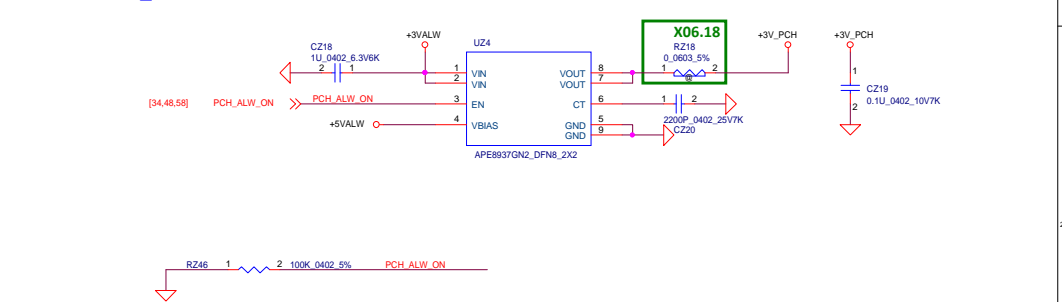
Alpine Ridge(TBT) Load Switch



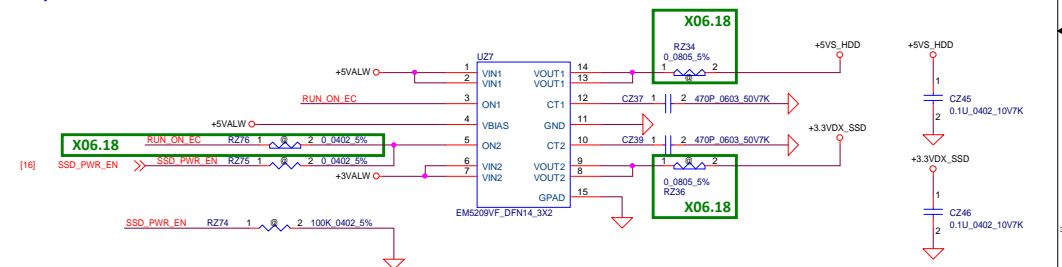
WLAN Load Switch



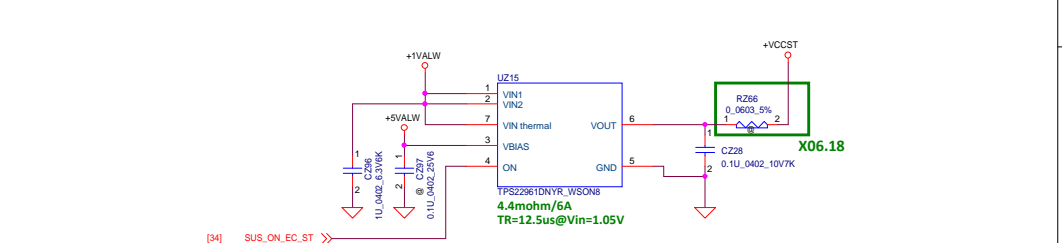
+3VALW to +3V_PCH



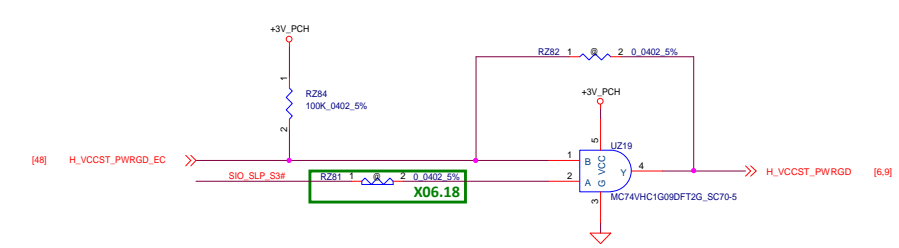
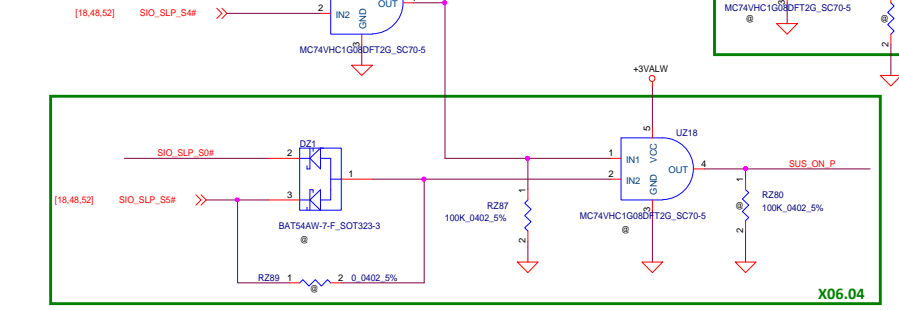
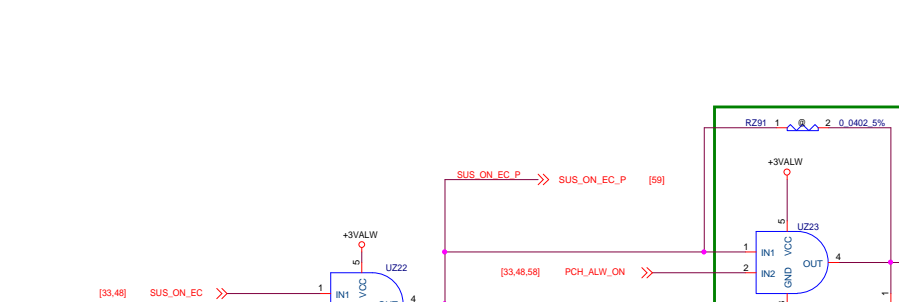
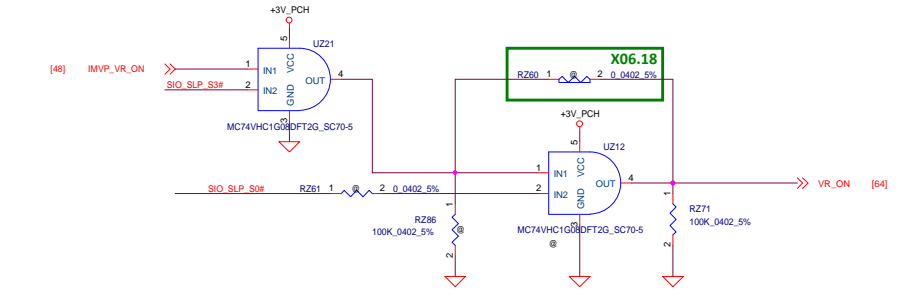
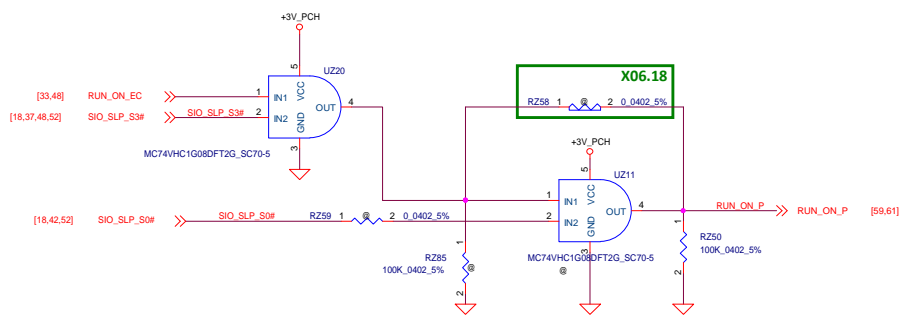
HDD, SSD Load Switch



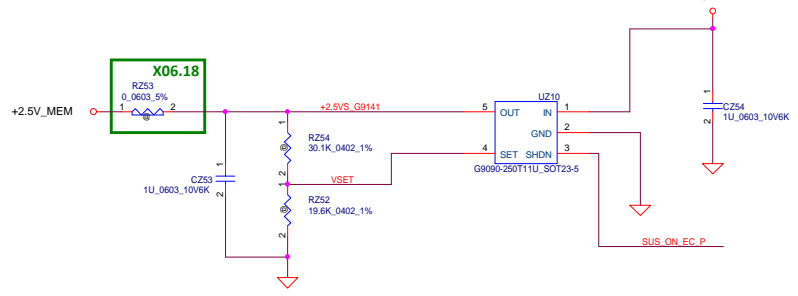
+VCCST Load Switch



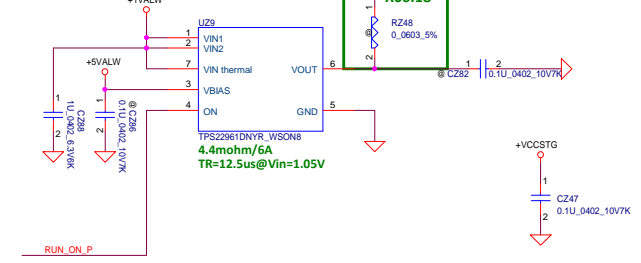
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SYS DC/DC Interface
Size				Document Number
Date				LA-C361P
Thursday, August 06, 2015				Sheet 33 of 71



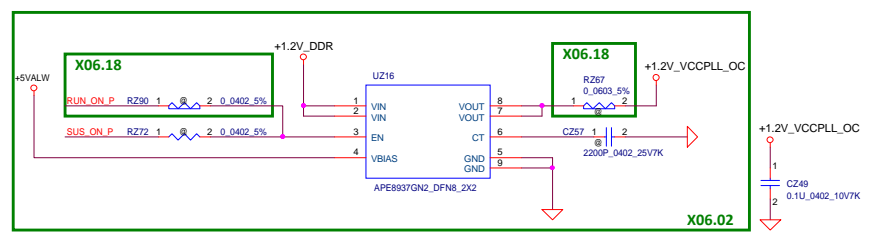
DDR4 VPP Load Switch



+VCCSTG Load Switch

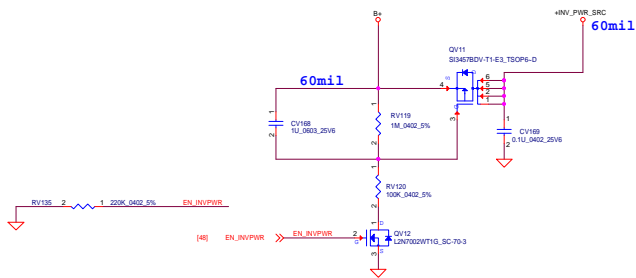


+VCCPLL_OC Load Switch

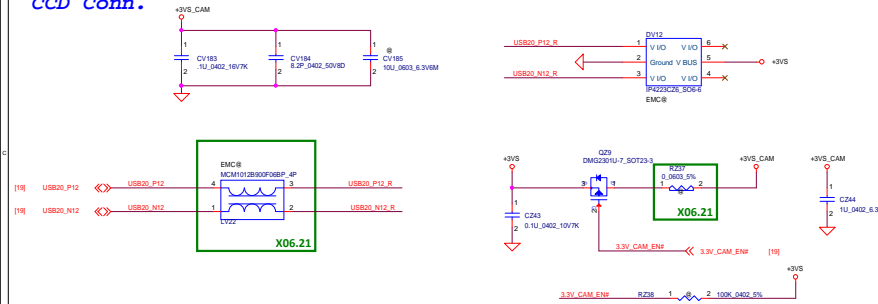


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				EC ENE-KB9012/ KC3810	
				Size	Document Number
				LA-C361P	Rev
				Date	Thursday, August 06, 2015
				Sheet	34 of 71

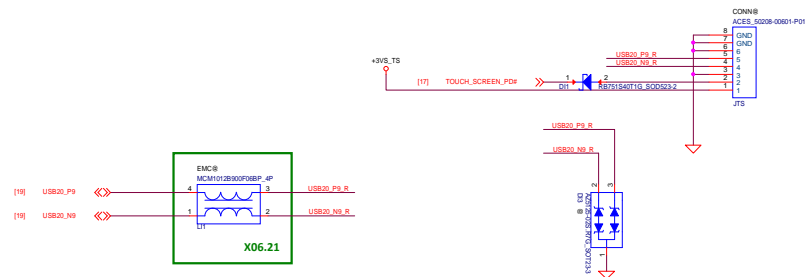
LCD backlight PWR CTRL



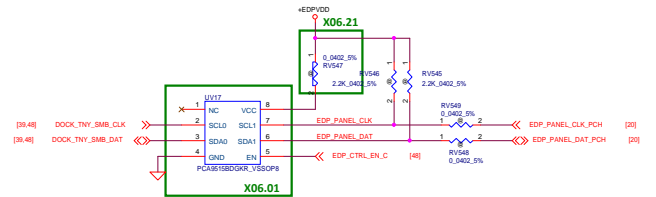
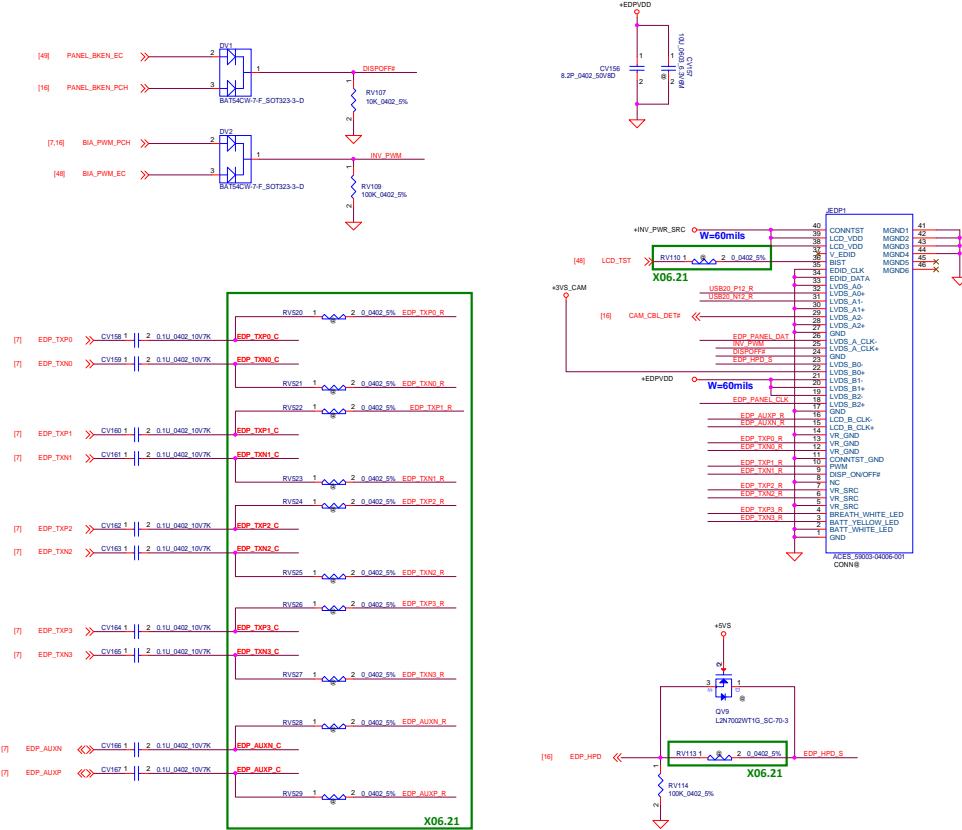
CCD Conn.



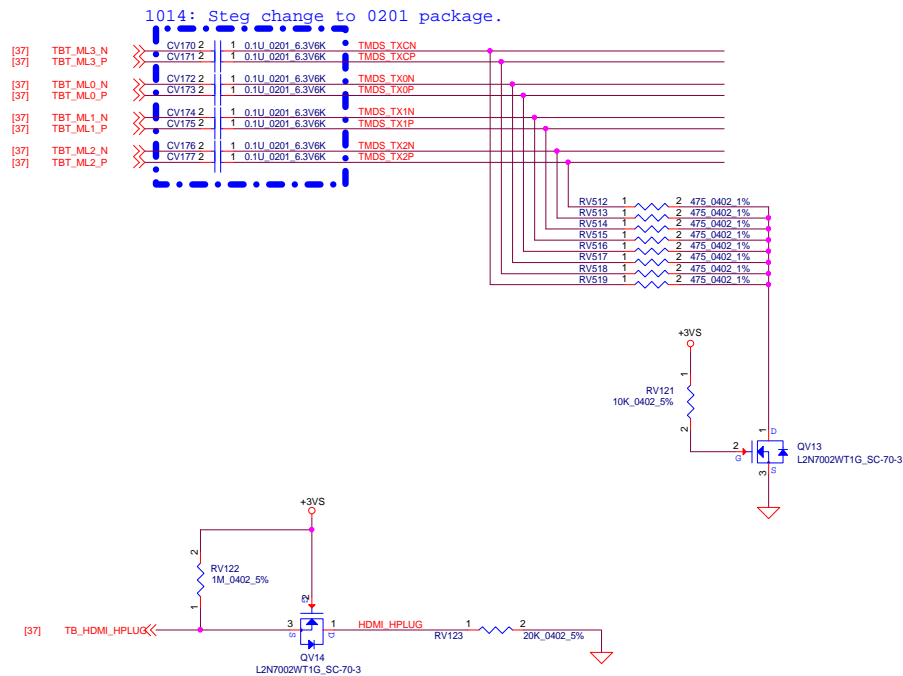
Touch Screen Conn.



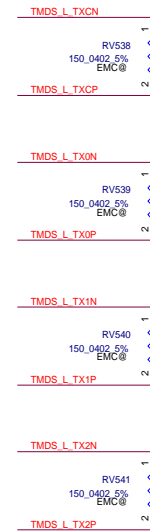
eDP & TS Conn.



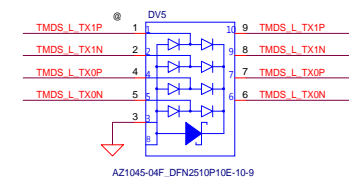
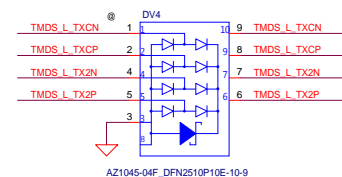
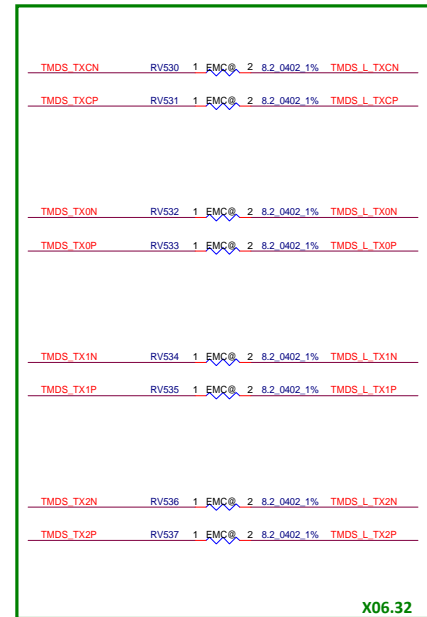
HDMI Active Level Shift(ALS type)



Place between ESD and CM-Choke

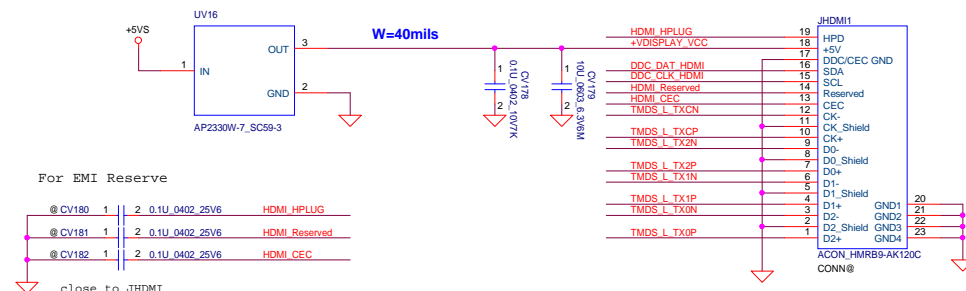


Place close to JHDMI1

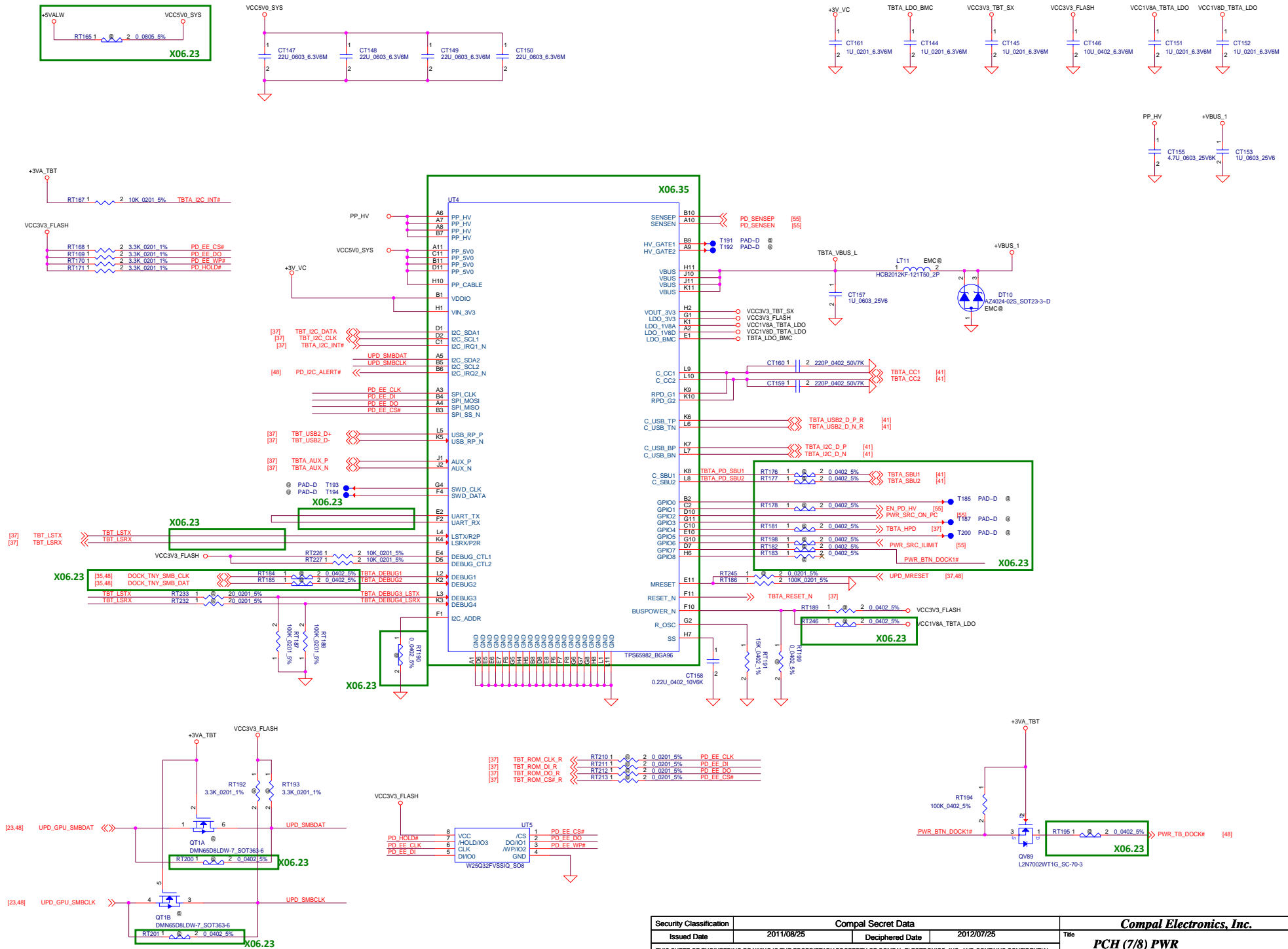


X06.32

HDMI conn

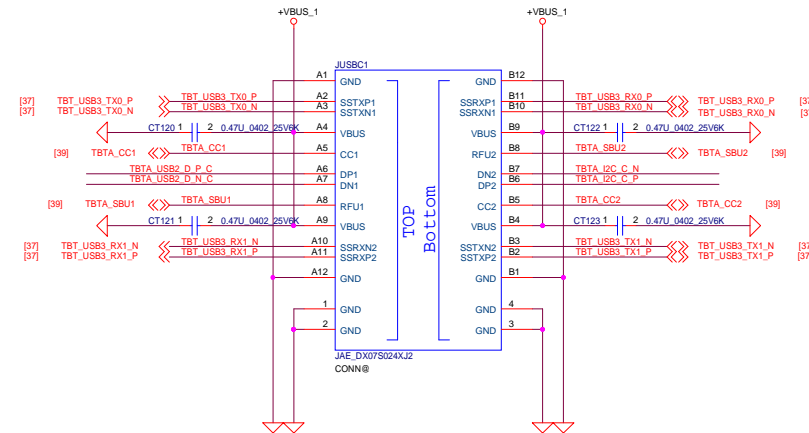
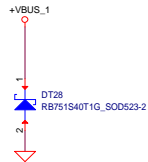
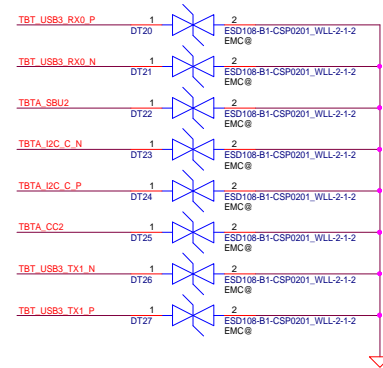
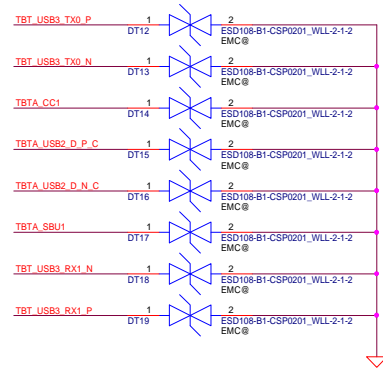
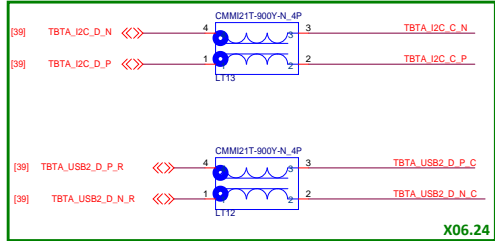


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2011/08/25	Deciphered Date	2012/07/25	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					HDMI		
					Size Custom	Document Number	Rev
					LA-C361P	0.1/000	
					Date	Thursday, August 06, 2015	Sheet 36 of 71

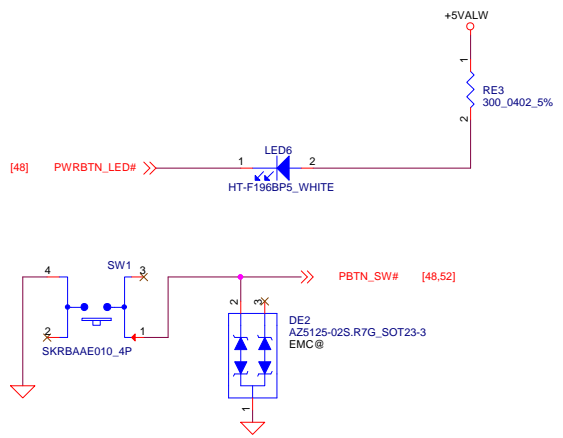


Reserve

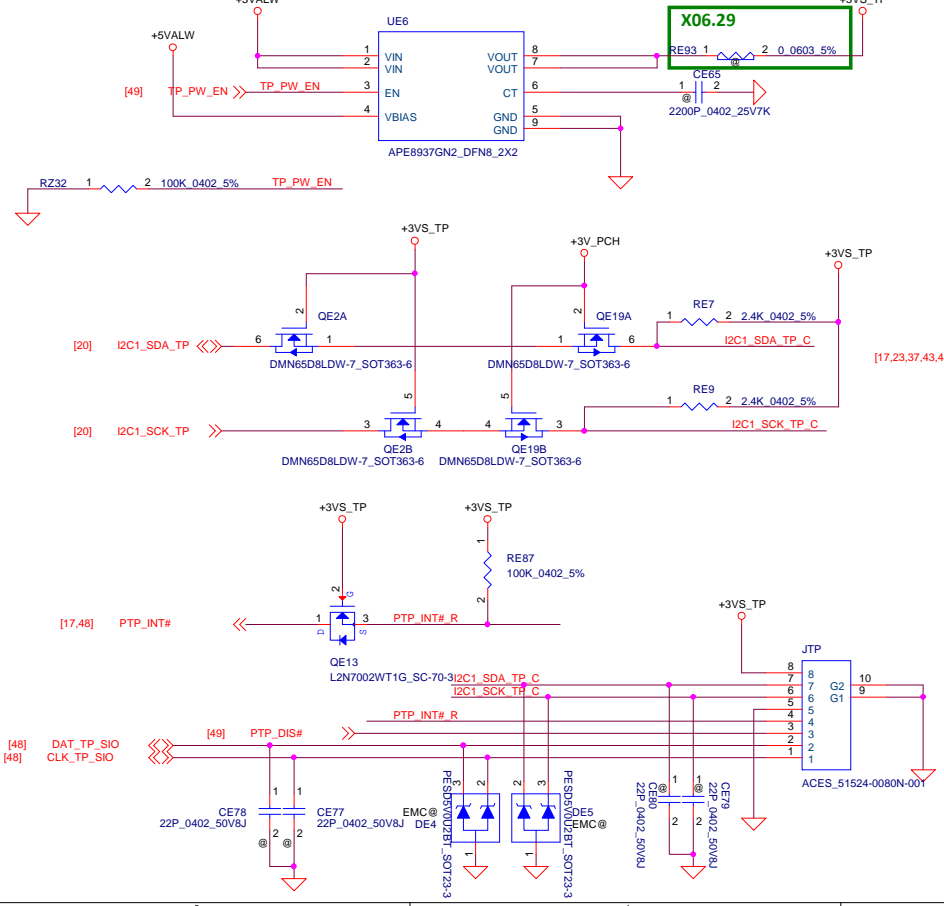
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Document Number	
2011/08/25		2012/07/25		Rev 0.1 (A00)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date: Thursday, August 06, 2015	
				Sheet 40 of 71	



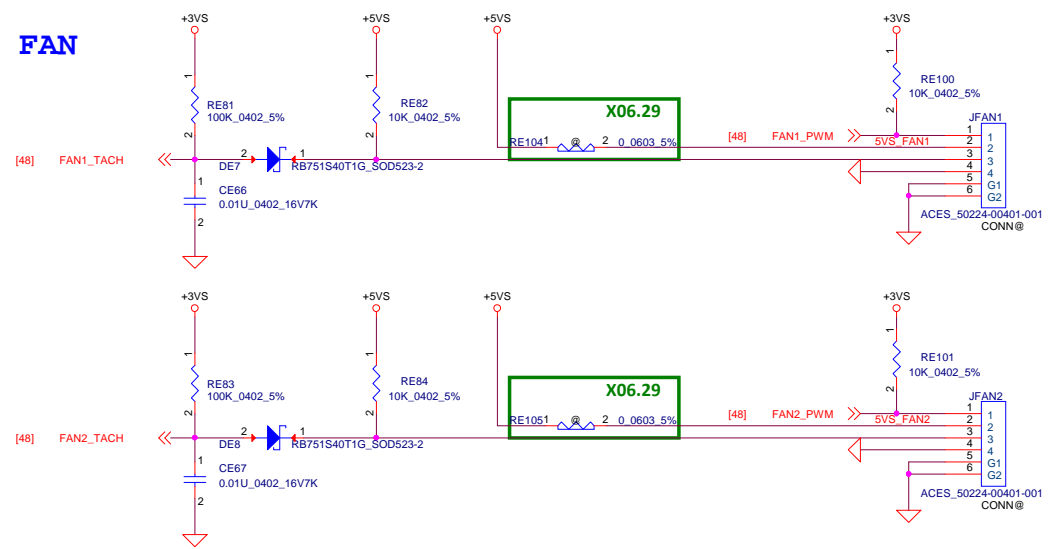
Power Button and LED



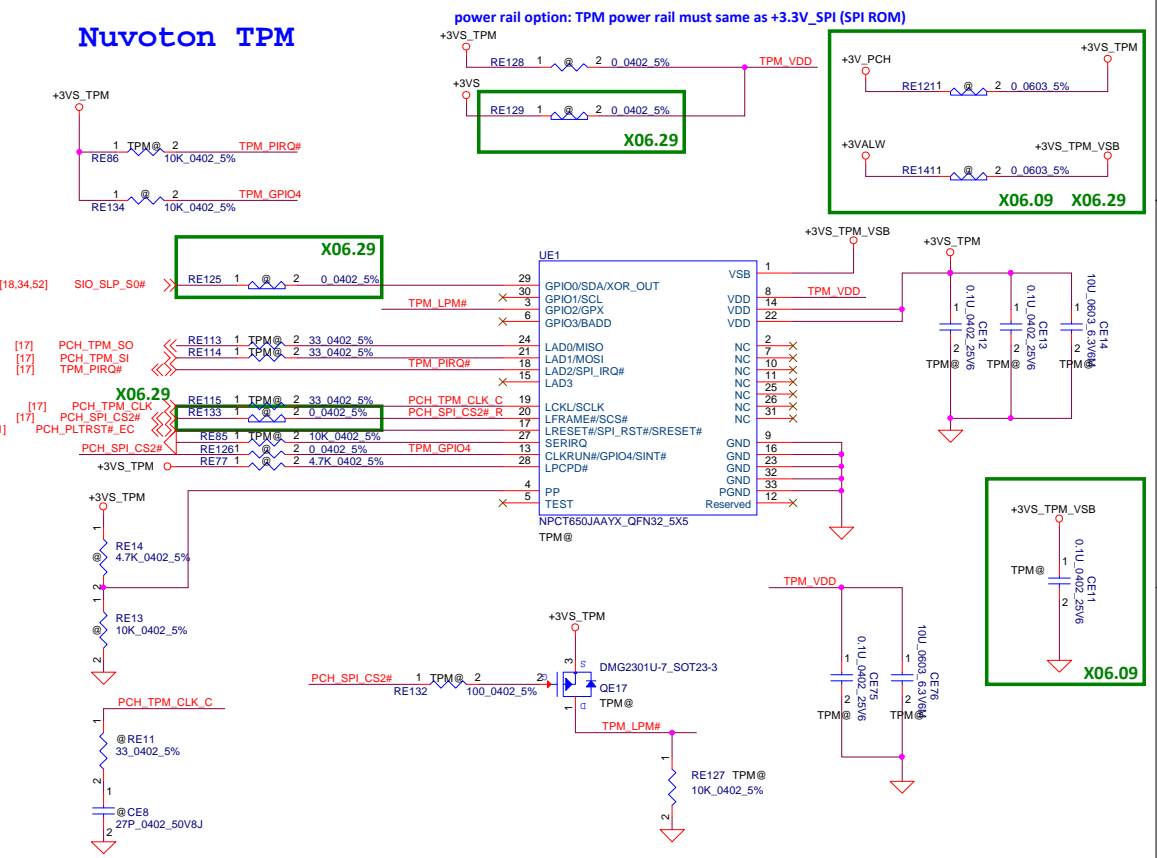
Touch pad



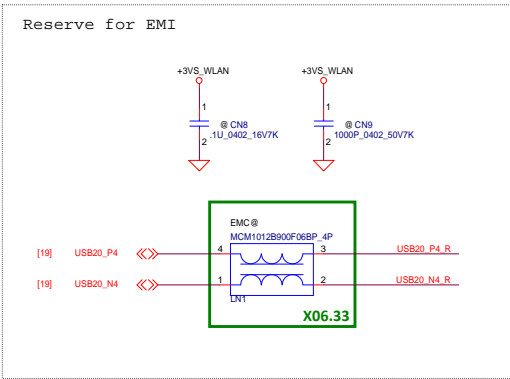
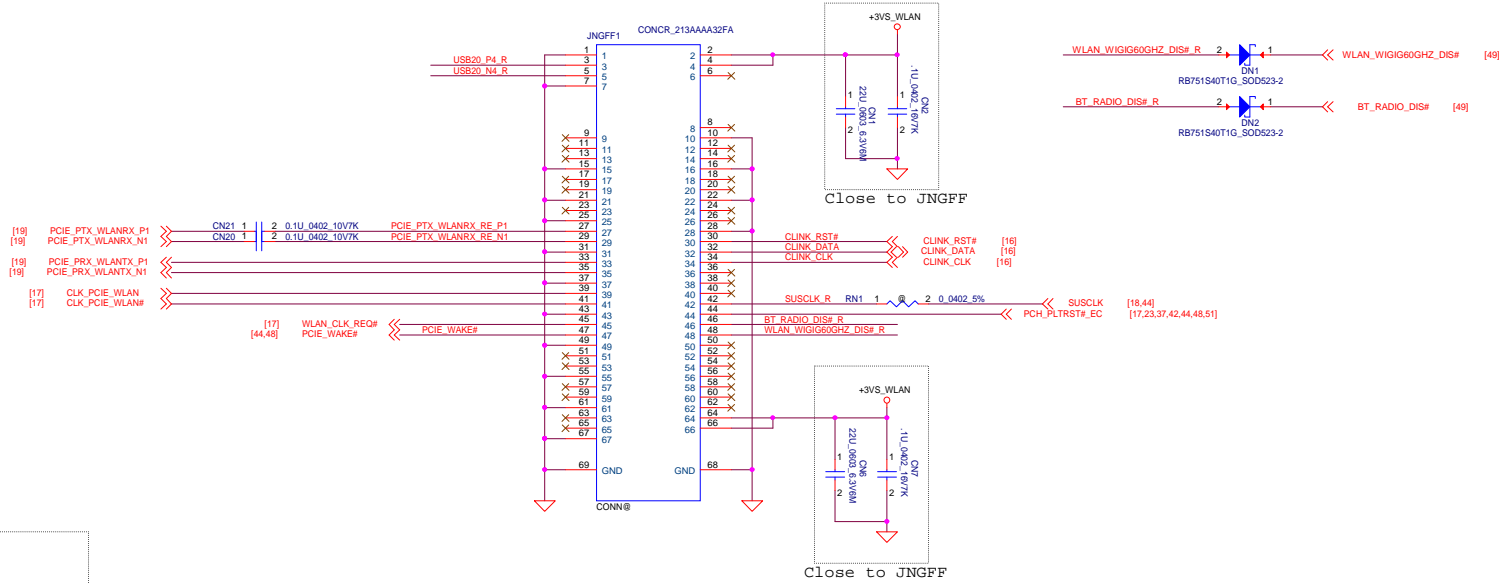
PWM FAN



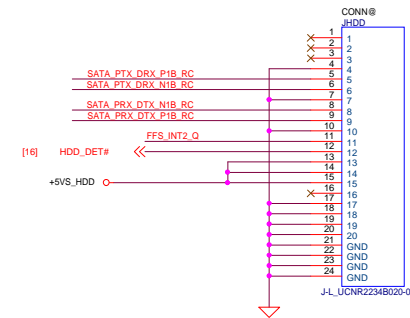
Nuvoton TPM



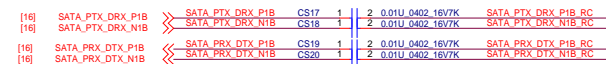
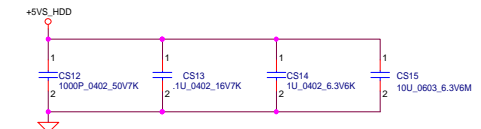
M.2 Slot-A Key-A (WLAN + BT)



HDD CONN

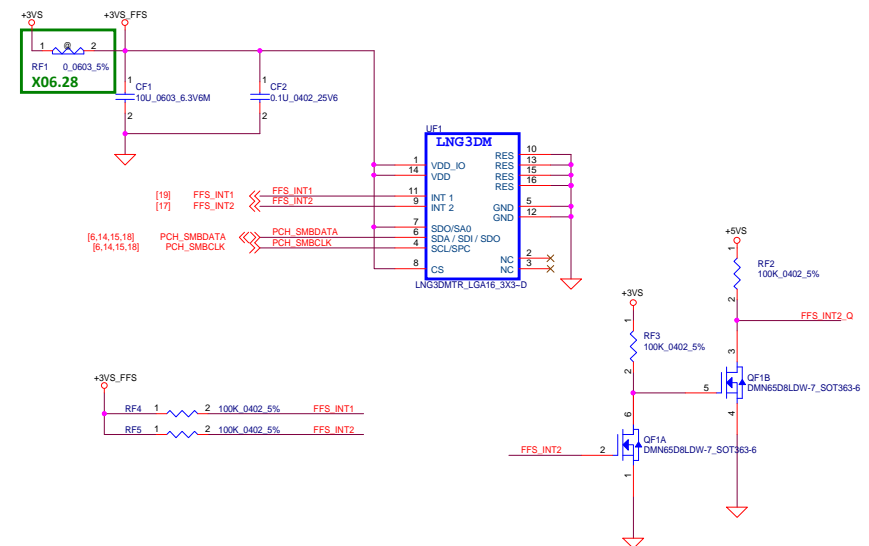


Place near HDD CONN (JHDD1)



BYPASS Circuit

Free Fall Sensor

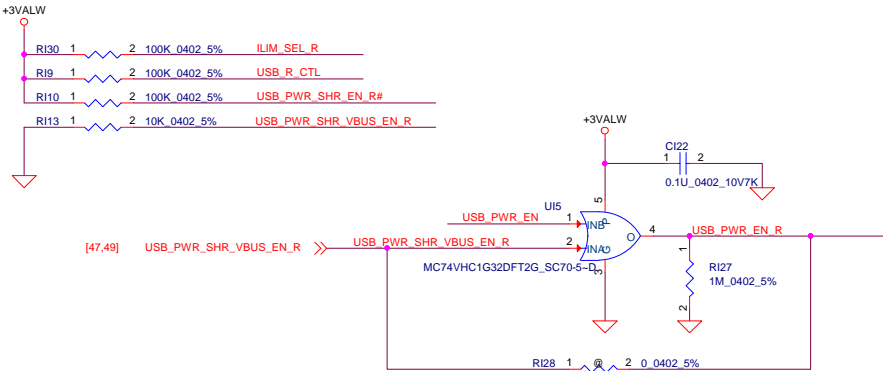


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/08/25		Deciphered Date	
				2012/07/25	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	
				DC/DC INTERFACE	
				Size	
				Document Number	
				LA-C361P	
				Date	
				Thursday, August 06, 2015	
				Sheet	
				45 of 71	
				Rev	
				0.1(000)	

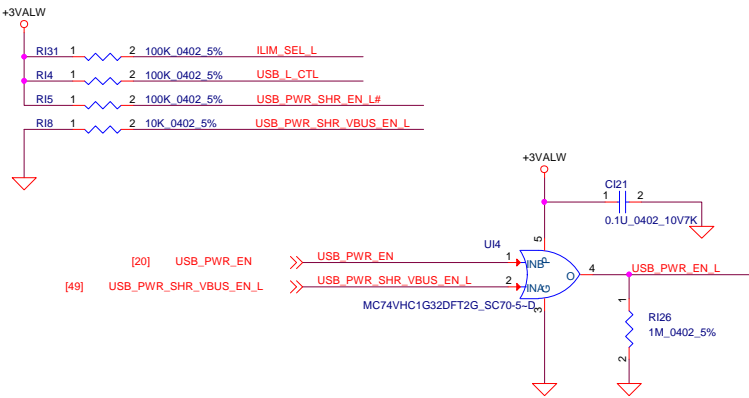
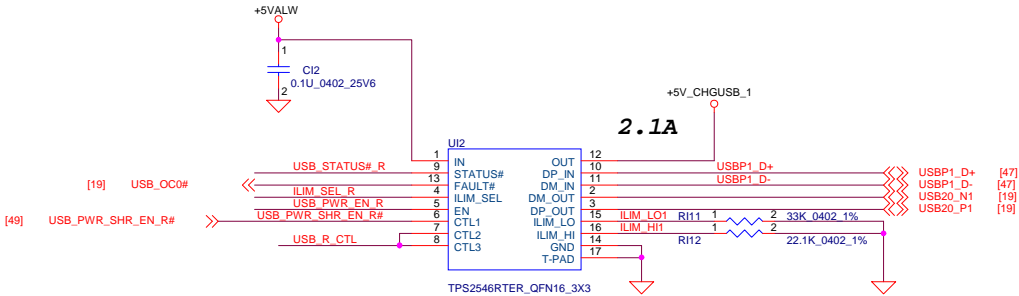
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

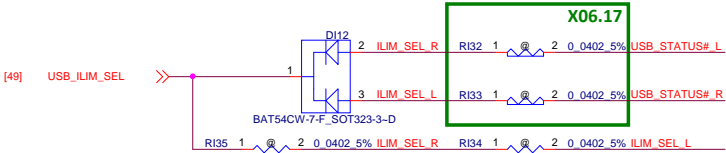
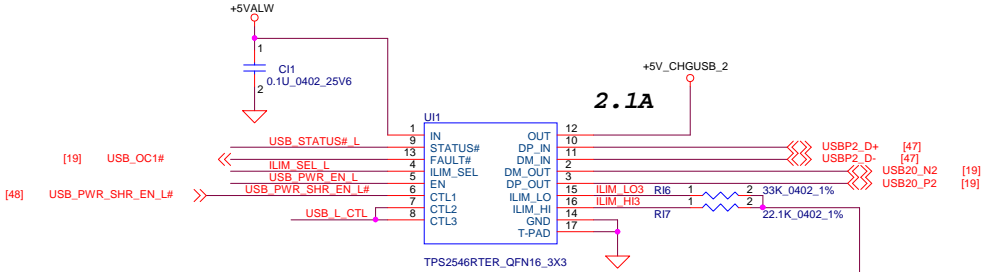
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)



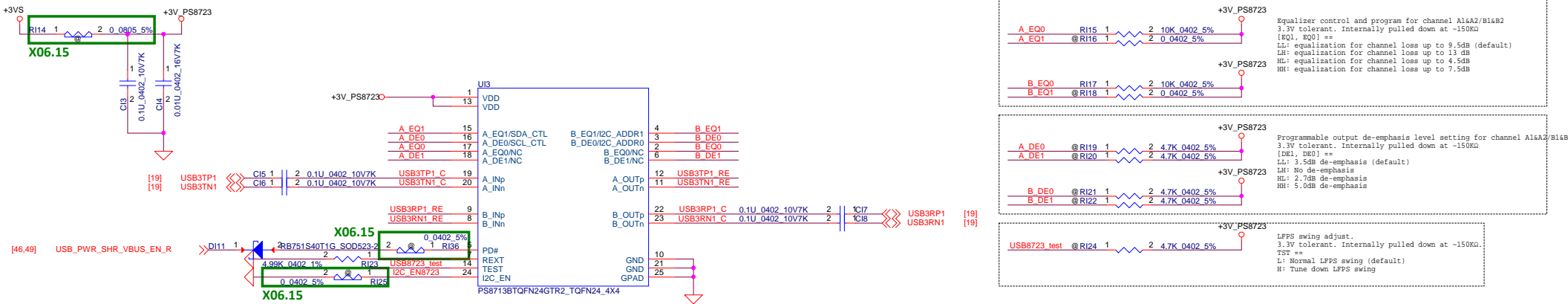
USB3.0 / USB2.0 Port1 (Right Side)



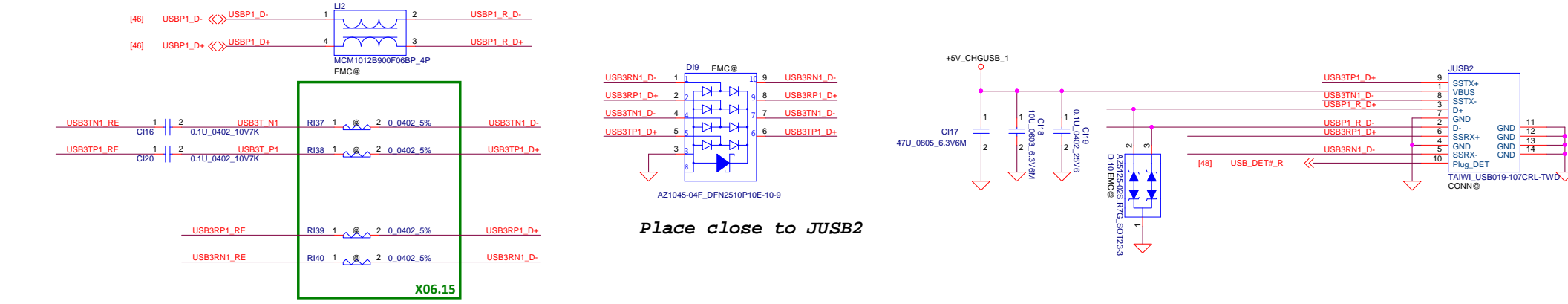
USB3.0 / USB2.0 Port2 (Left Side)



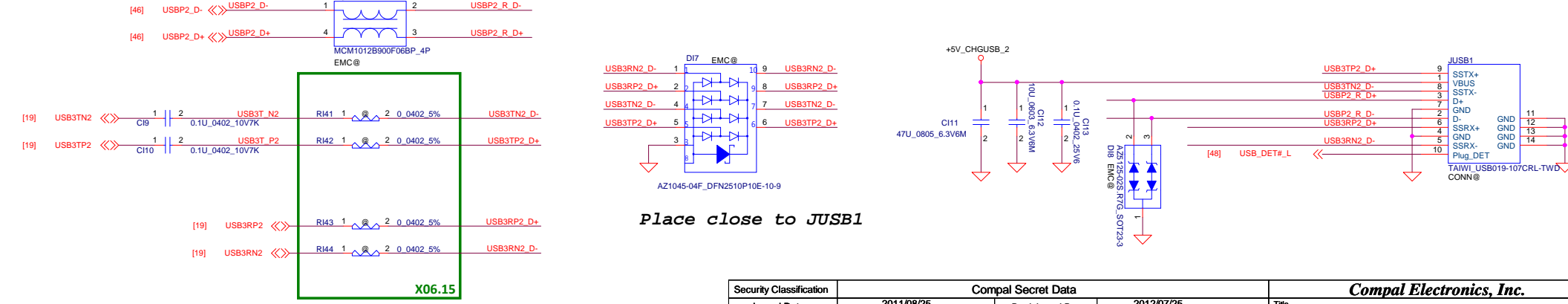
USB3.0 Re-driver

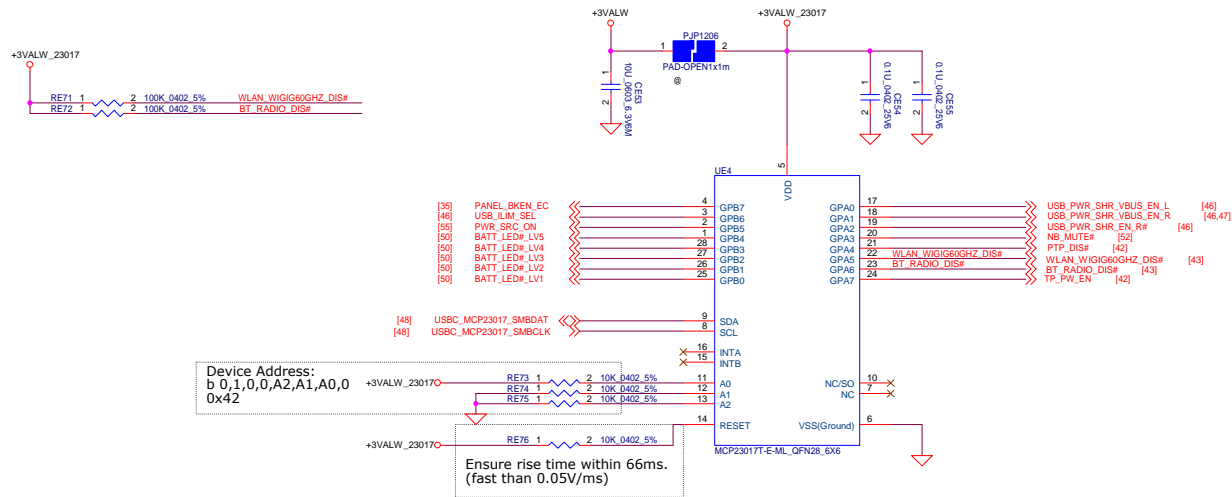


USB3.0 / USB2.0 Port1 (Right Side)



USB3.0 / USB2.0 Port2 (Left Side)

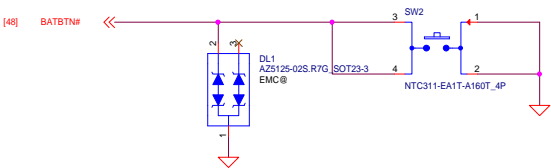




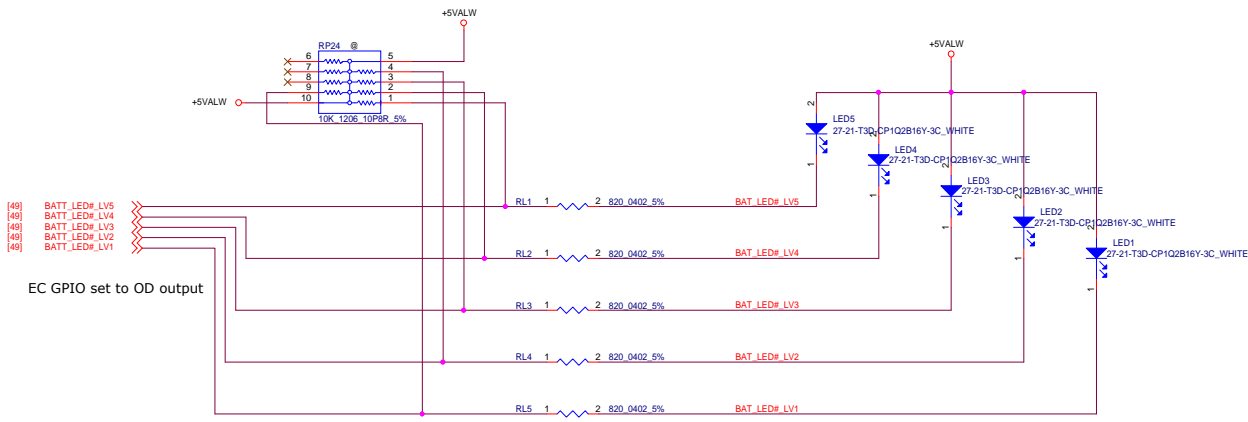
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/08/25	Deciphered Date	2012/07/21	Title
					AMP TPA3113/SPK conn.
Size	Document Number	LA-C361P			Rev
C					0.1(200)
Date: Thursday, August 06, 2015		Sheet 49 of 71			

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

BATT LED Power Button

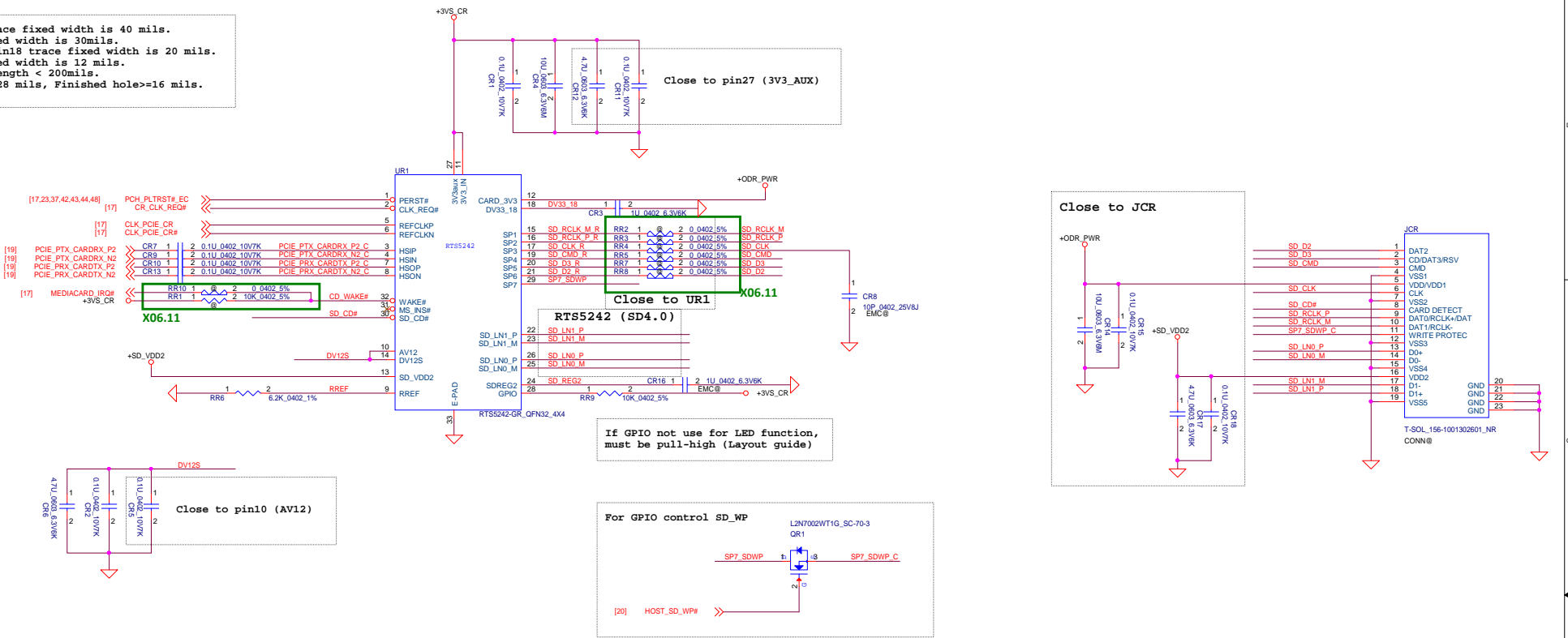


Battery Gauge LED

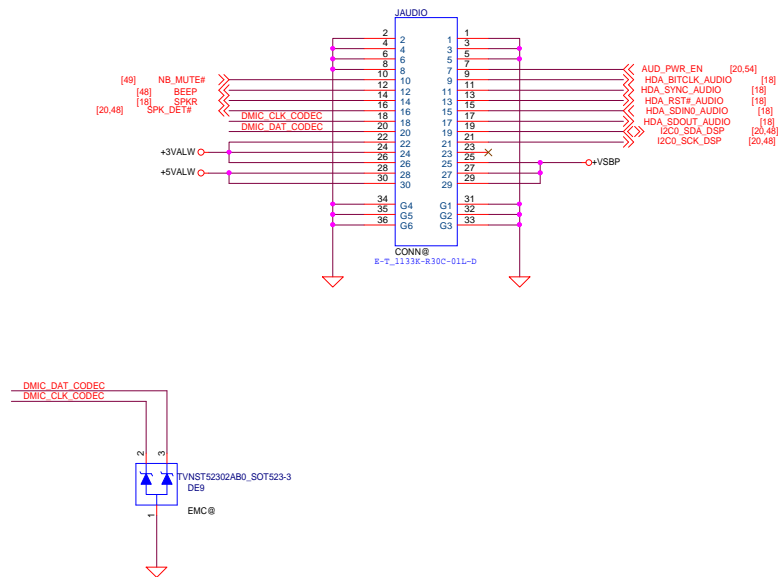


Card Reader

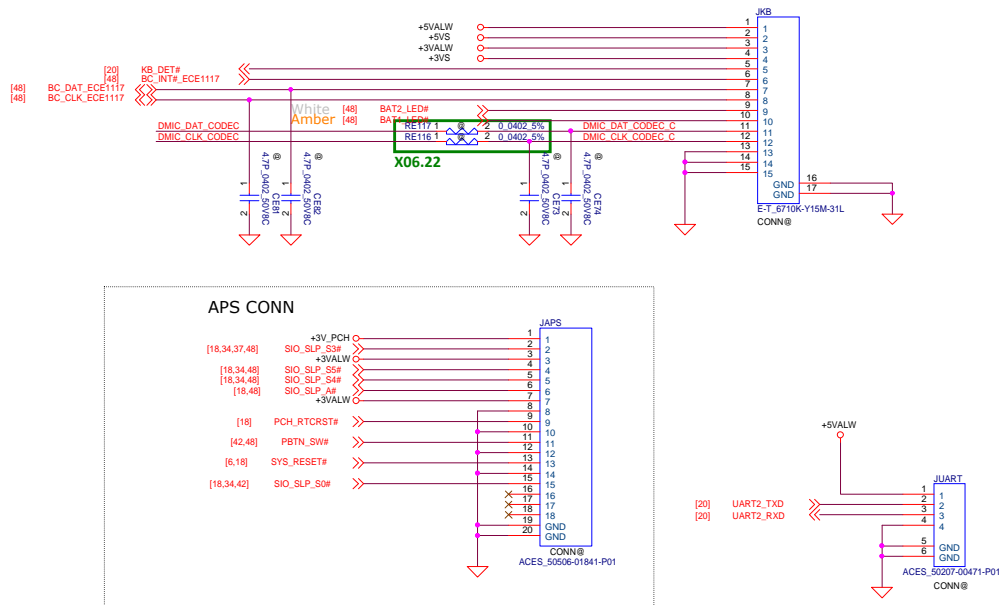
Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



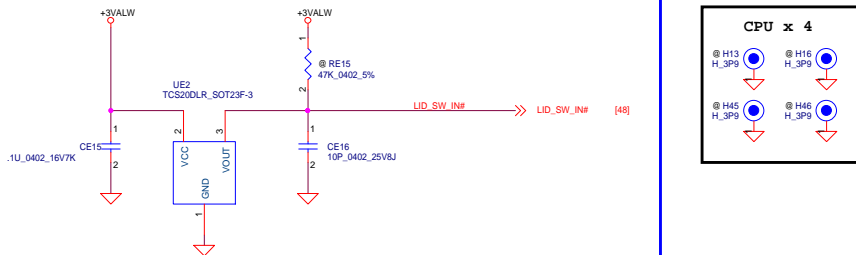
AUDIO Board Conn.



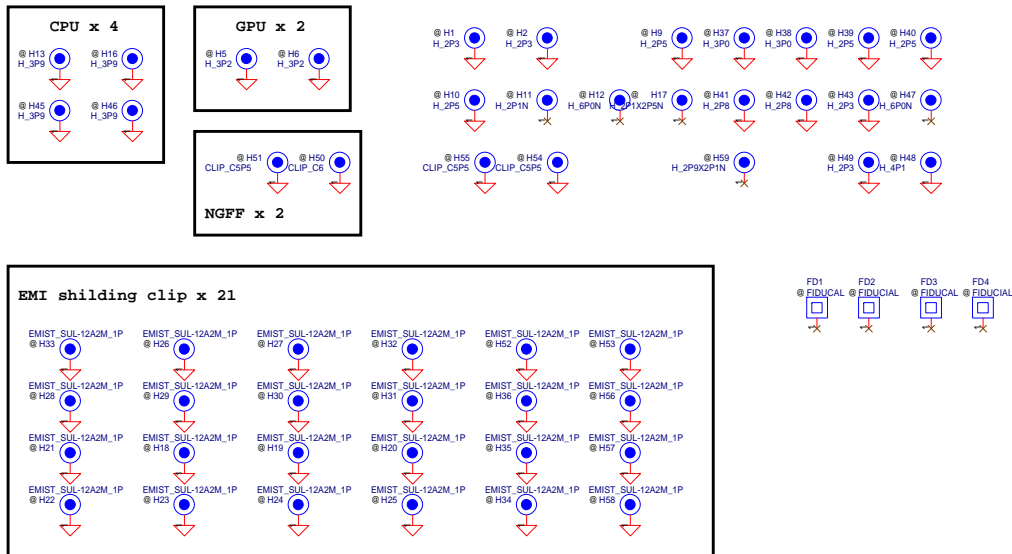
Keyboard Controller board + DMIC



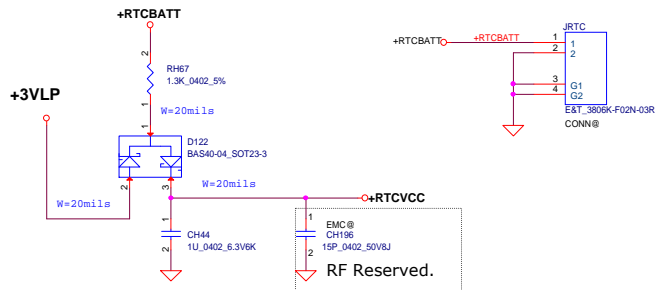
Lid Switch



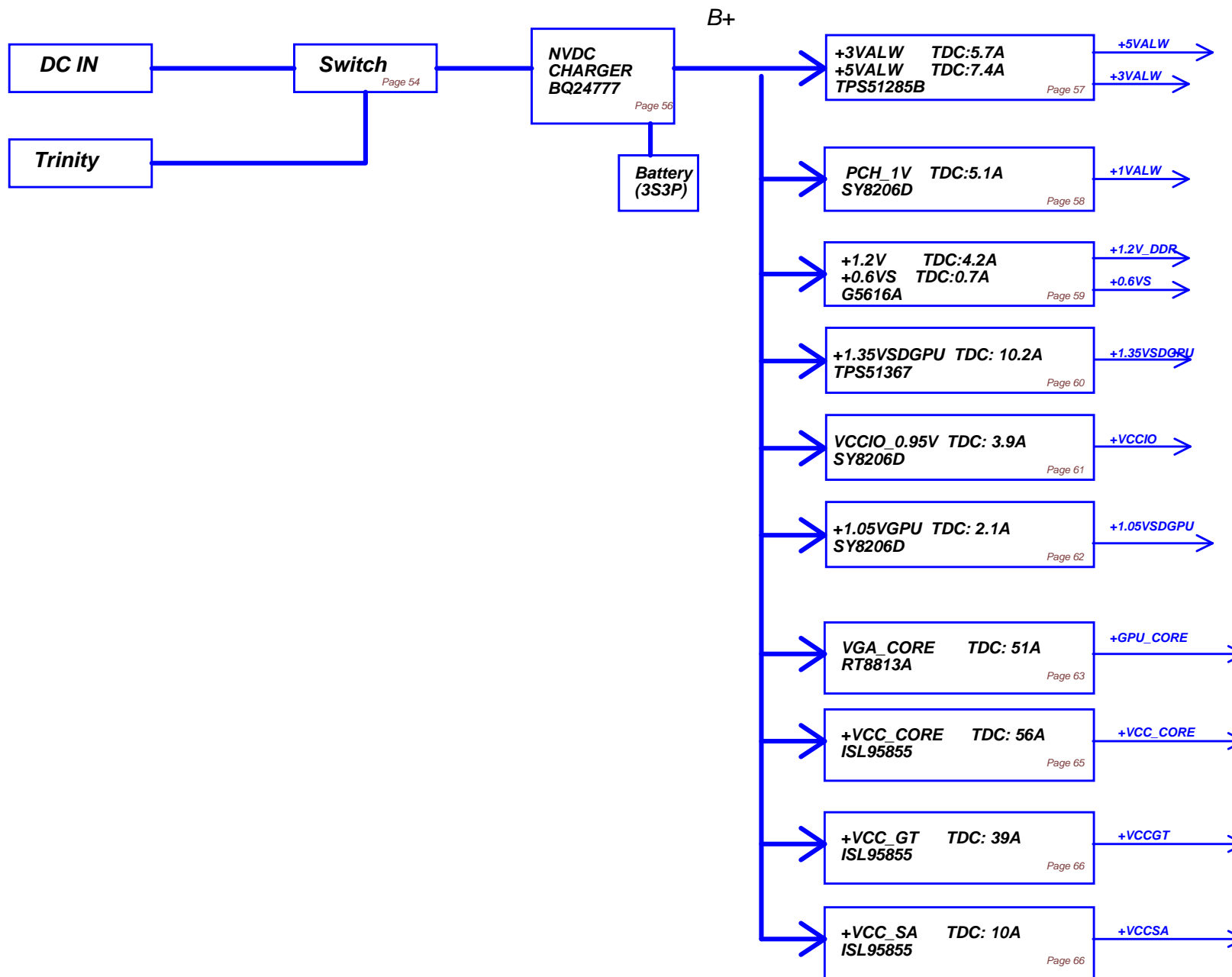
Screw Hole

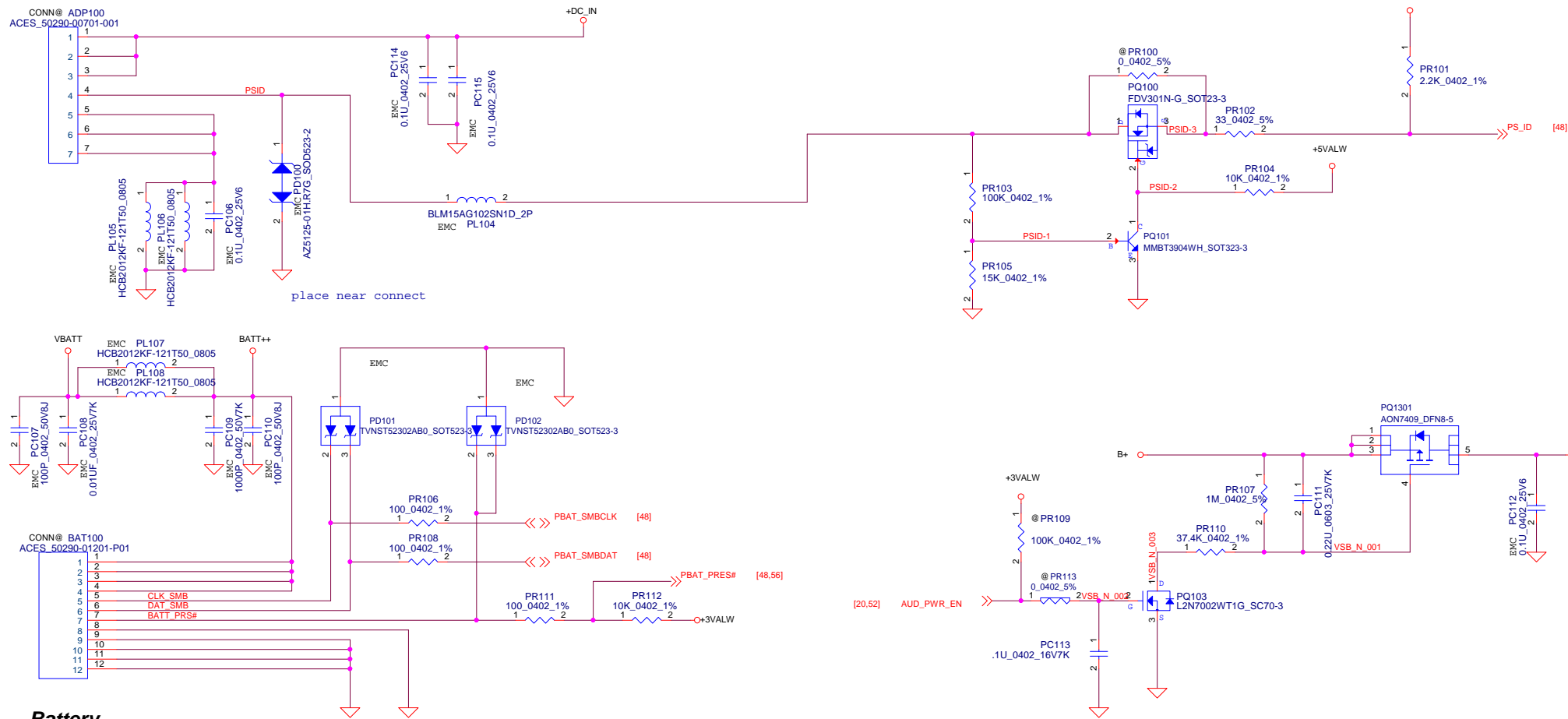


RTC Battery With Charge Function



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				LA-C361P
				Rev
				0.1(200)
				Date
				Thursday, August 06, 2015
				Sheet
				52 of 71





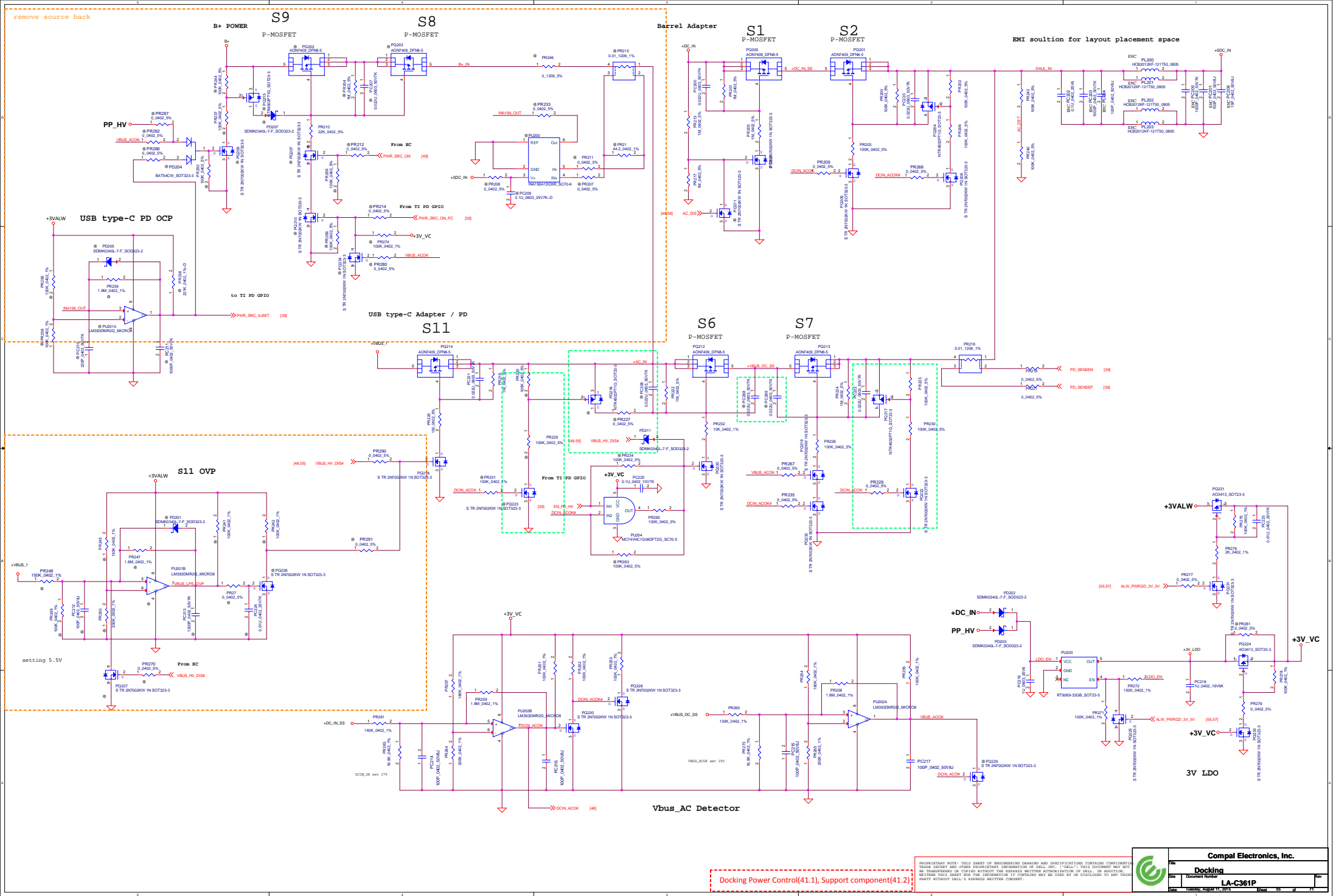
Smart Adapter circuit (39.1)

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

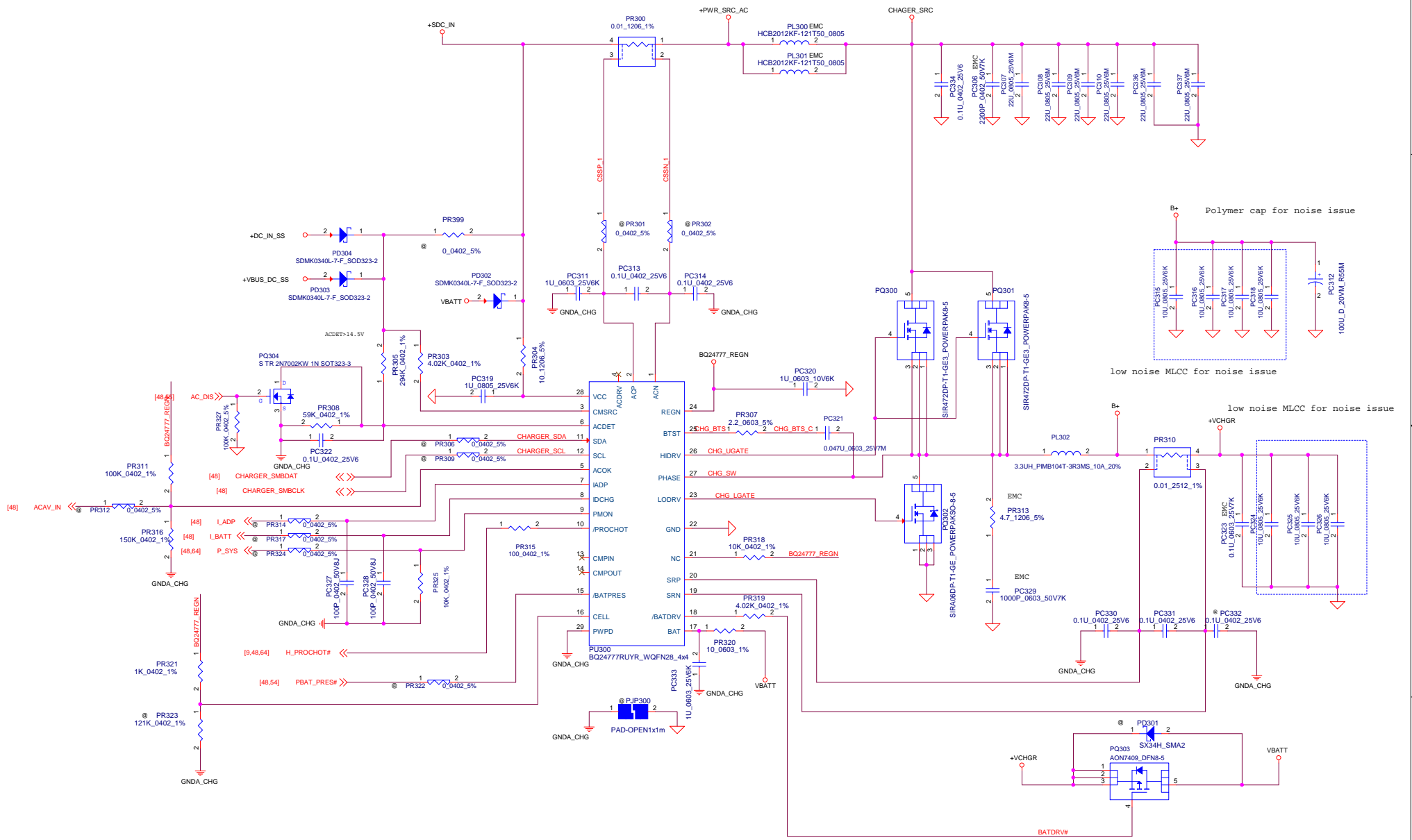


Compal Electronics, Inc.

Title		
PWR-DCIN / BATT CONN / OTP		
Size	Document Number	Rev
	LA-C361P	0.1(00)
Date:	Tuesday, August 11, 2015	Sheet 54 of 71




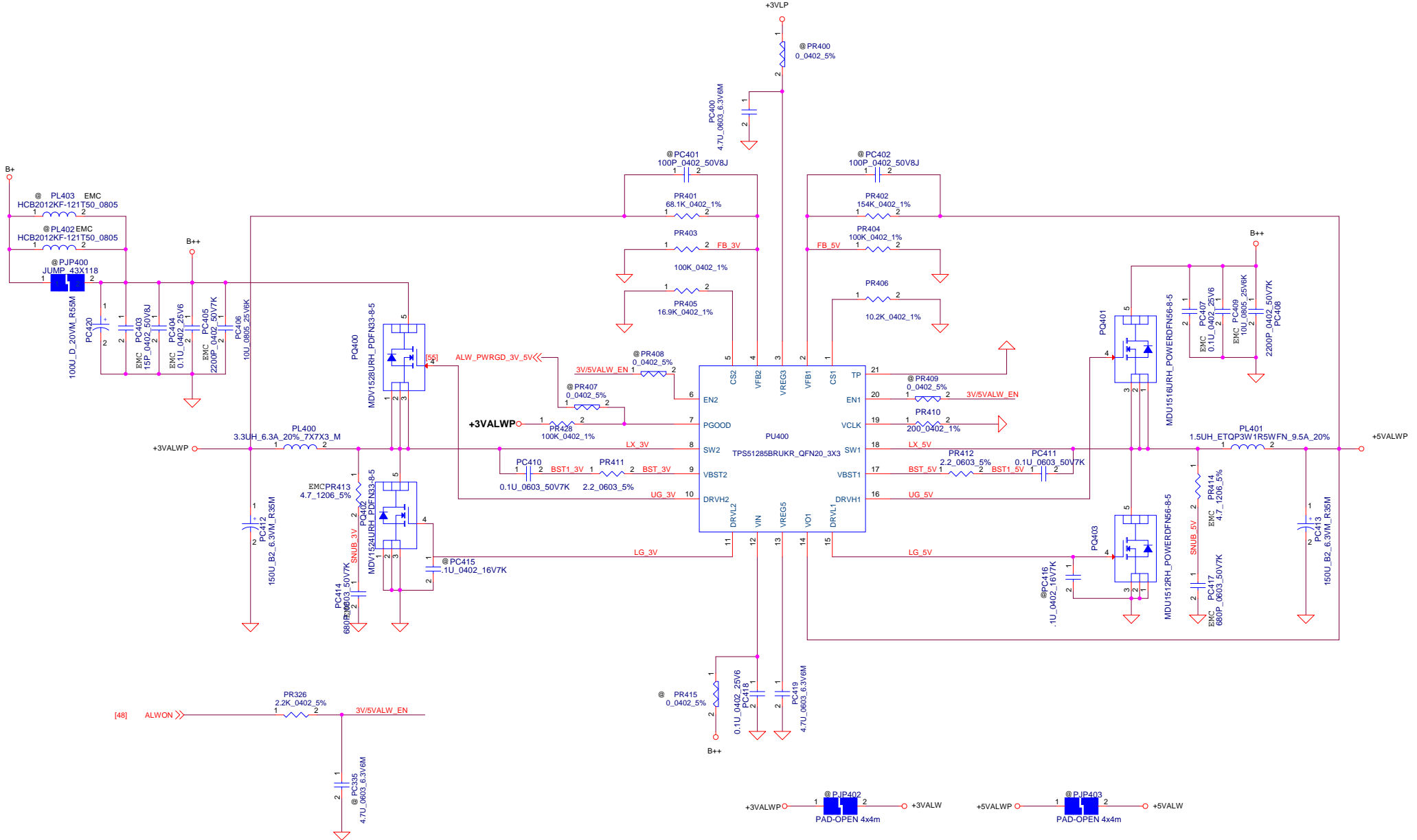
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRETS AND OTHER PROPRIETARY INFORMATION OF DELL EMC ("DELL"). THIS DOCUMENT MAY NOT BE TRANSMITTED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, WITHIN THIS SHEET THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



Charger controller(40.1), Support component(40.2)

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSMITTED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY OTHER PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

				Compal Electronics, Inc.			
Title		Charger					
Size		Document Number					
Date		Rev		LA-C361P			
Sheet		56		of 71			

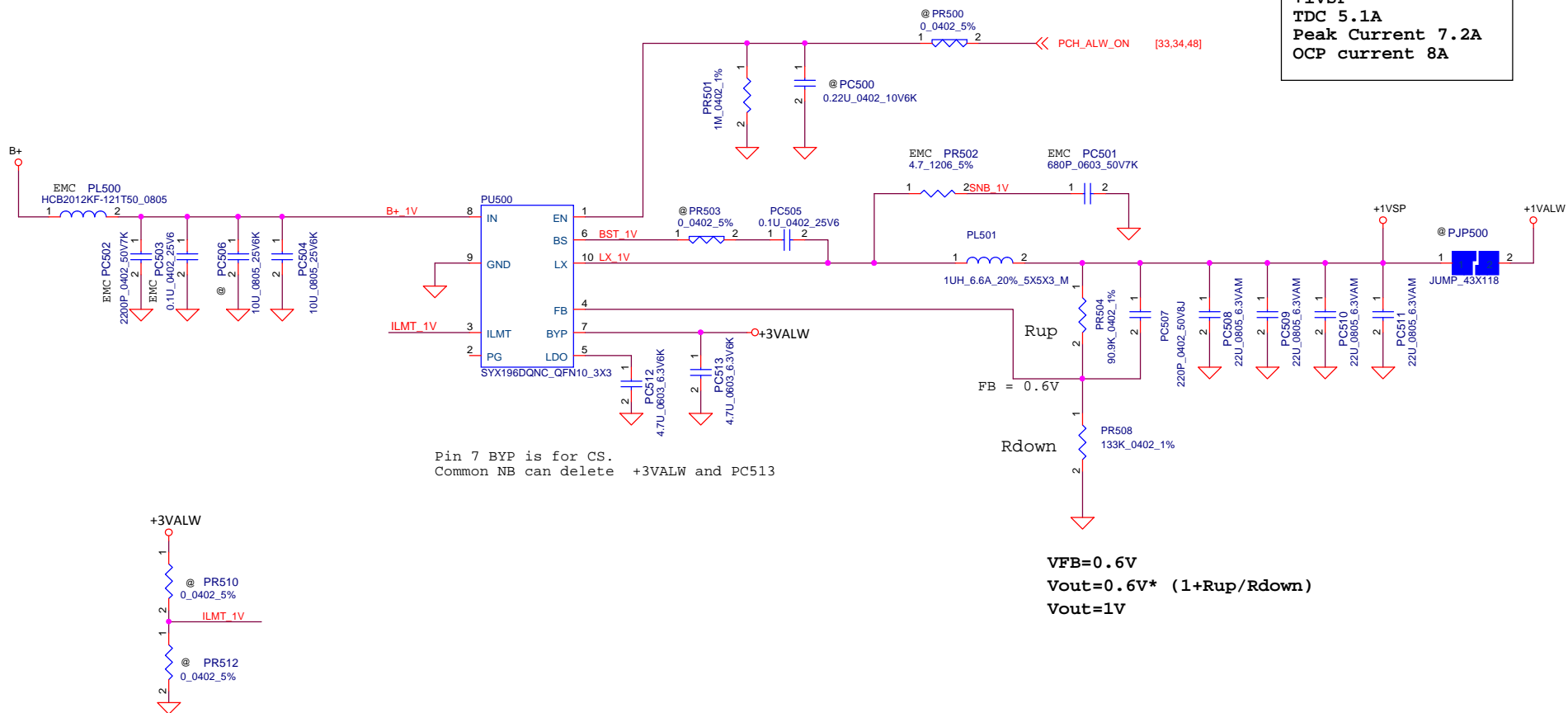


3.3VALWP
TDC 5.7A
Peak Current 8.1A
OCP current 9.7A

5VALWP
TDC 7.4A
Peak Current 10.5A
OCP current 12.6A

3V/5V controller(35.1), Support component(35.2)

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



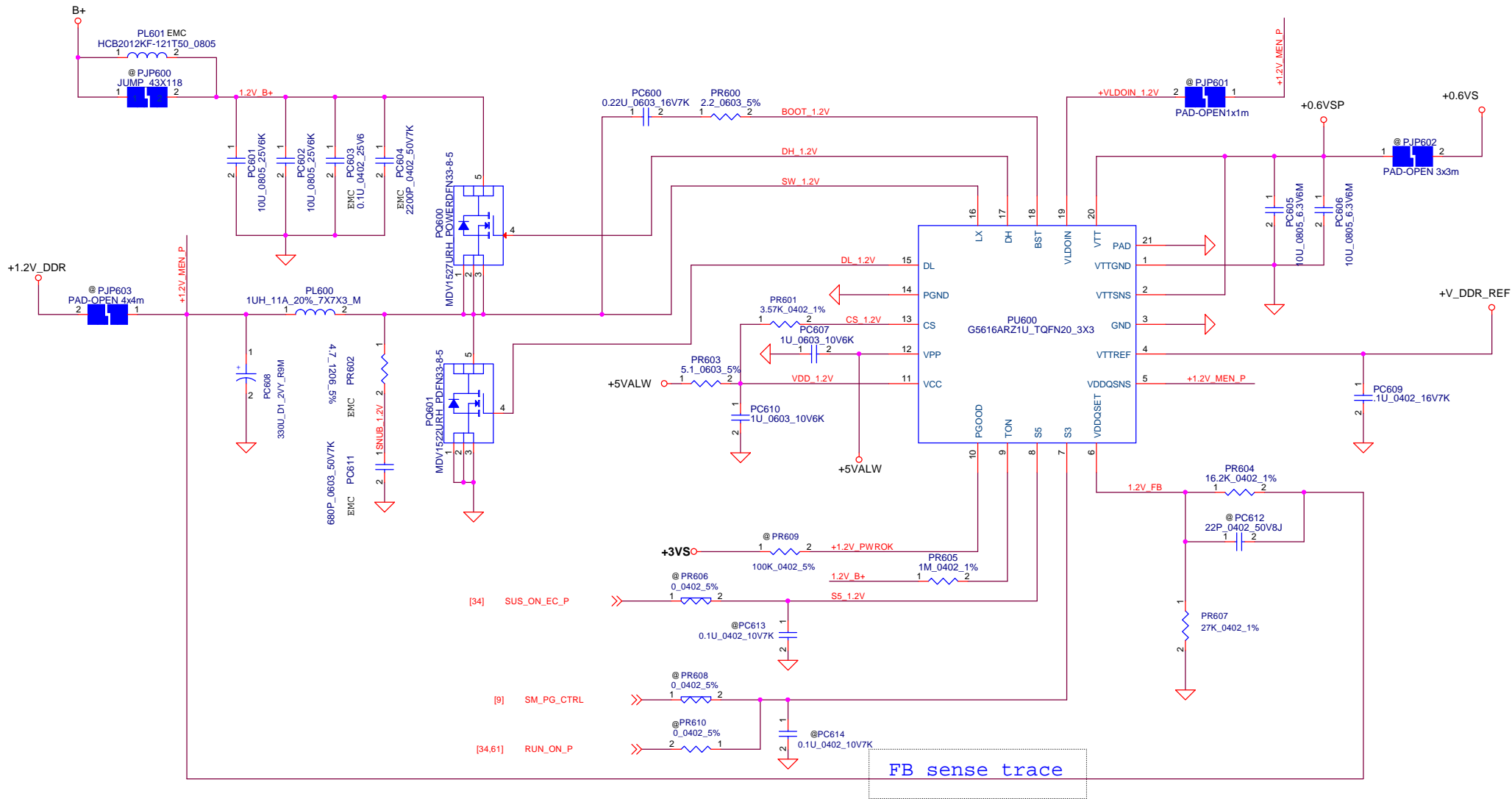
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC513

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1V

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +IVA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-C361P
				Date:	Tuesday, August 11, 2015
				Sheet	58 of 71



1.2Volt +/- 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A

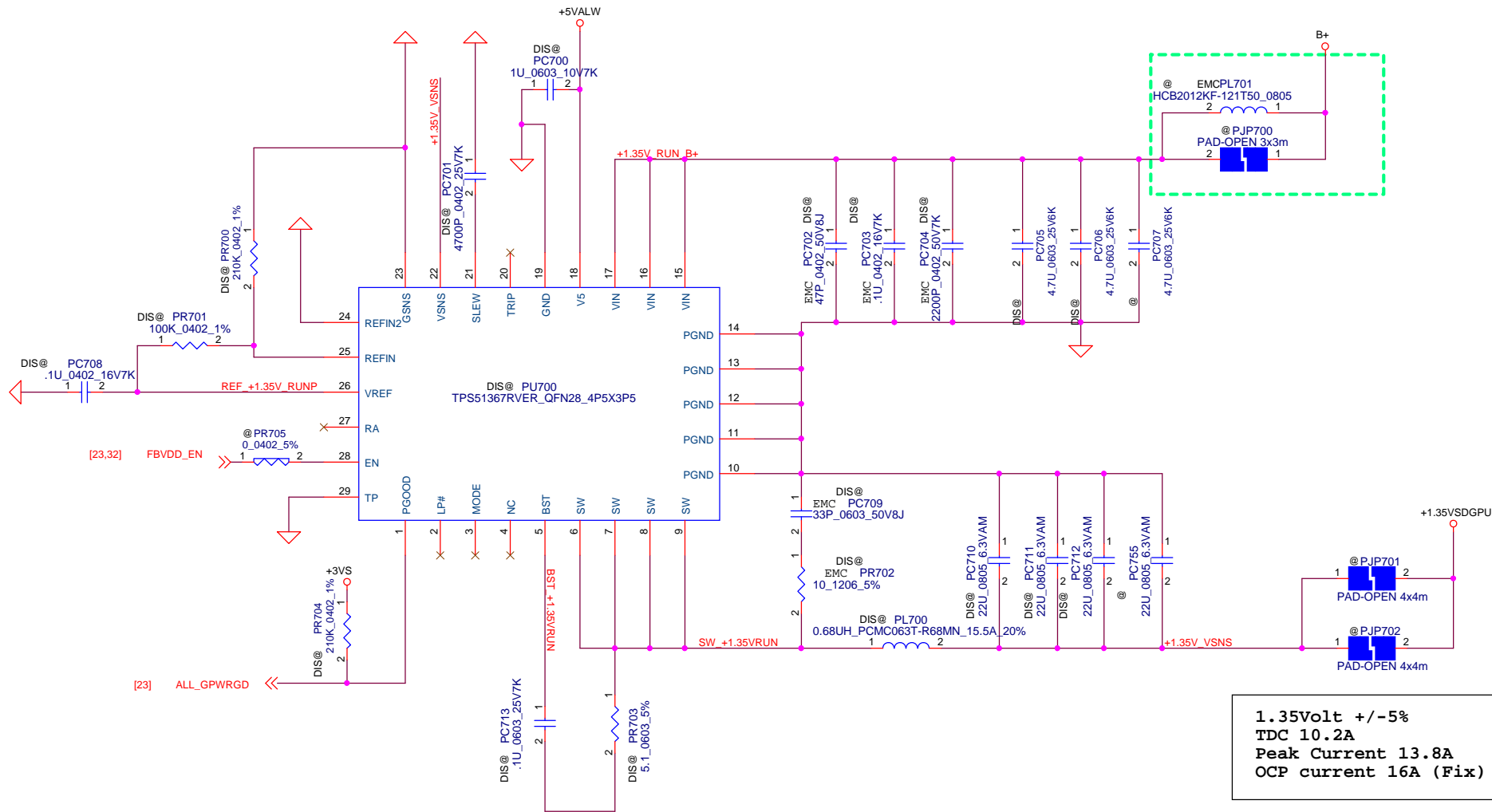
0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

DDR controller(35.3), Support component(35.4)

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title		+1.35V_MEN/+0.675V_DDR_VTT	
Size	Document Number	LA-C361P	
Date	Tuesday, August 11, 2015	Sheet	59 of 71

Rev 1.0(400)



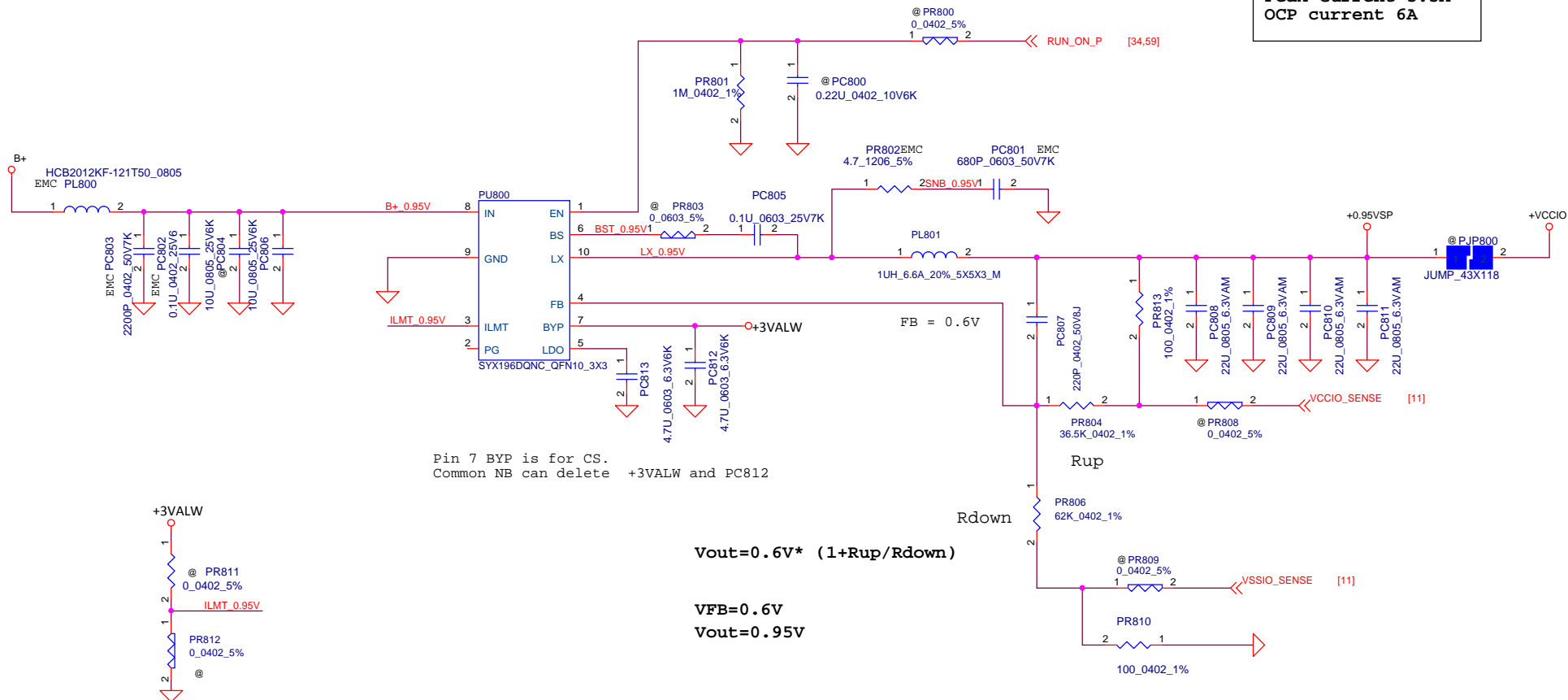
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.			
Title			
PWR_+1.5VDGPU			
Size	Document Number		Rev
	LA-C361P		1.0(400)
Date:	Tuesday, August 11, 2015		Sheet 60 of 71



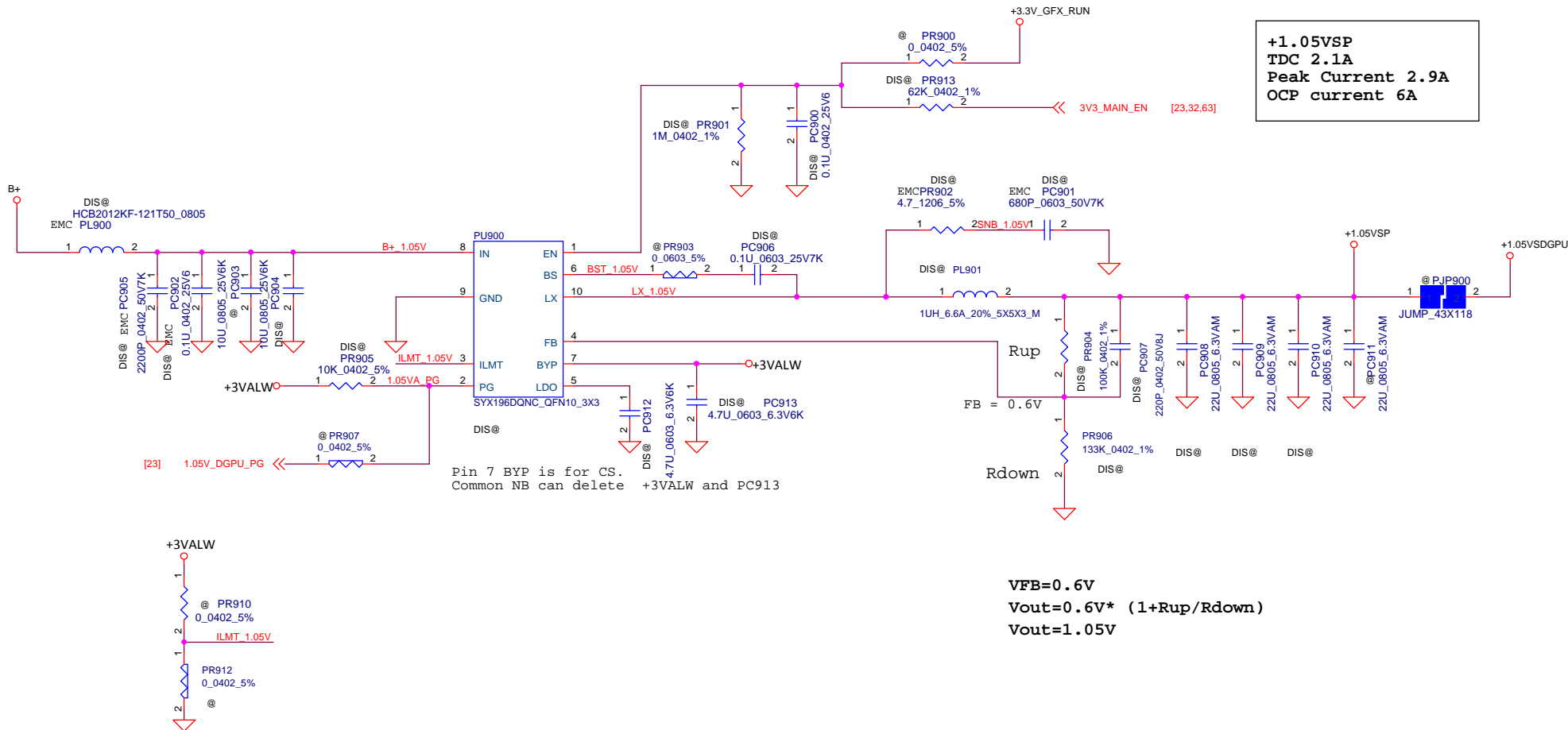
DDR controller(35.3), Support component(35.4)

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



1.05V controller(35.5), Support component(35.6)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +0.95VA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-C361P
				Date:	Tuesday, August 11, 2015
				Sheet	61 of 71



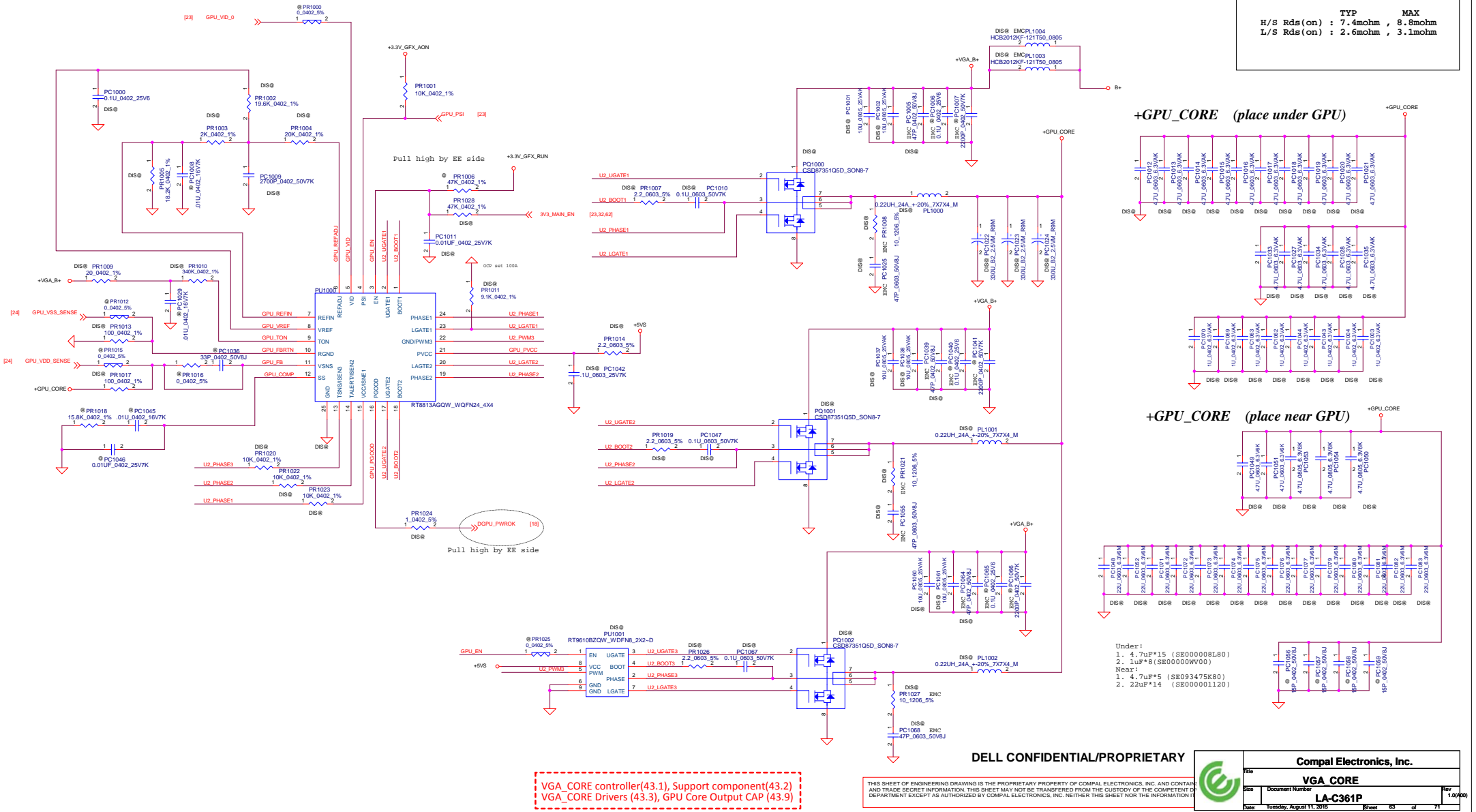
The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

GPU other power_Regulatorr(43.7), Support component(43.8)

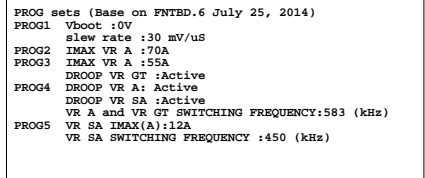
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +1.05VA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-C361P
				Date:	Tuesday, August 11, 2015
				Sheet	62 of 71
				Rev	0.1

GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%

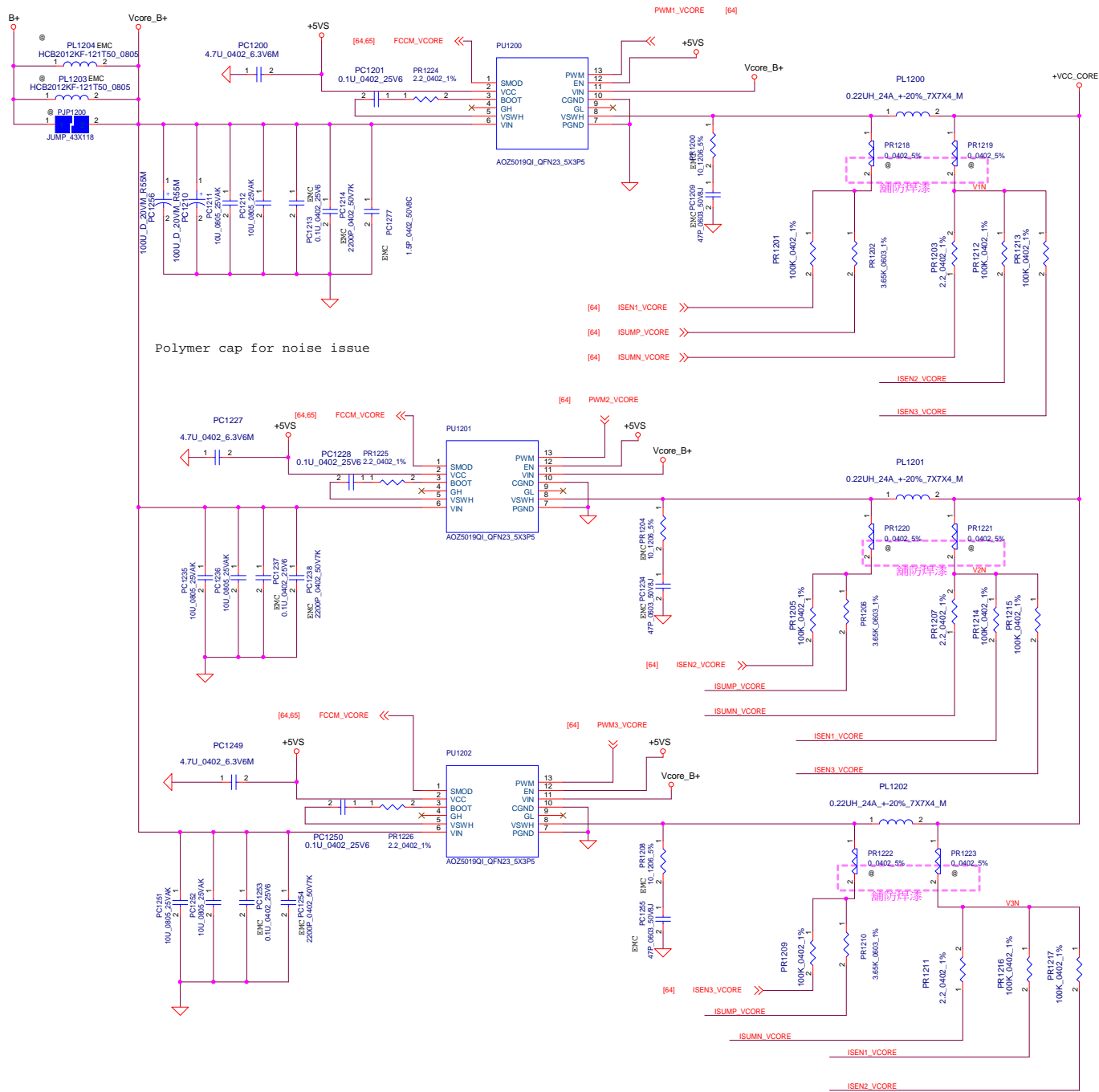
TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm



Compal Electronics, Inc.	
VGA CORE	
LA-C361P	
File	Rev
Size	Document Number
Date	Thursday, August 11, 2016
Sheet	83 of 91



Title			
<Title>			
Size	Document Number	Rev	
Custom LA-C361P		<RevCode>	
Date:	Tuesday, August 11, 2015	Sheet	64 of 71



Polymer cap for noise issue

VCC_core (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):56A
 Peak Current 68A
 DC Load line ~1.8mV/A
 AC Load line ~1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3), CPU_Core output CAP(36.4), Acoustic Noise B+ Bulk CAP(37.2)

Title	<Title>		
Size	Document Number	Rev	
C	LA-C361P	<RevCode>	
Date:	Tuesday, August 11, 2015	Sheet	65 of 71

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, de-POP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the same power rail	Change RH571 power rail from +3VS to +3V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIQ_S08 to W25Q128FVSIQ_S08	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Change RZ58 connection from UZ11.2 to UZ11.4, Change RZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit for useless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH194,CH195. Delete net MPHPY_PWR_EN, move RZ70 to page 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UTS from W25Q80BLZPIG_WSON8 to W25Q80DVSSIQ_S08,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC3V3_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBT. Add RT198 to PWR_SRC_ILIMIT.Swap UT4.B2/C2 net. Update RT165 from 1206 to 0805, RT167,RT168, RT169,RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT192,RT192,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net	X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	UPD_SMBDAT/UPD_SMBCLK"	X01
8	18	PM	2014/12/15	EE	Update RE67 to 62K	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	modify for support deep sleep function	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	change Power rail for correct design	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Add pull high resistor for MB side	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Change GPIO for sync common GPIO table	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Pin swap for DFB review	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add RPH34 replace to RV520,RV521,RV522 and add net THERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Add pull high resistor by vendor request	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB XDP design	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Follow CRB boardfile	Change net BID_BC to GPP_C15, Add Net UARTT0_TX from GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Modify Debug UART from closed Chassis to Open Chassis	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Change PU resistor follow Miramar	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add 2 PAD for ME NUT	Add RE111 43K series SIO_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Add series resistor follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Change BOM to follow CRB	Add RE112 and Connect net BID_DIS to UE3.A10, swap Net BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update BOM for design change	Change JNGFF1 to CONCR_213AAAA32FA	
26	18	PCH	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change RP21 to RH576,RH577,RH578,RH579. Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change array resistor to resistor for routing	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, USB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USB_DET_EC_R#	
28	18	TS	2014/12/18	EE	Change net name by EC request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Update Touch Screen Connector by ME request	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Add Pull down resistor for USB2.0	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Reserve test point for Alpine Ridge	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete common mode chok & ESD for vendor feedback	Delete QE14	
33							
34							
35							
36							
37							
38							
39							

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
20				EE			X01
21				EE			X01
22				EE			X01
23				EE			X01
24				EE			X01
25				EE			X01
26				EE			
27				EE			
28				EE			
29				EE			
30				EE			
31				EE			
32				EE			
33				EE			
34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			